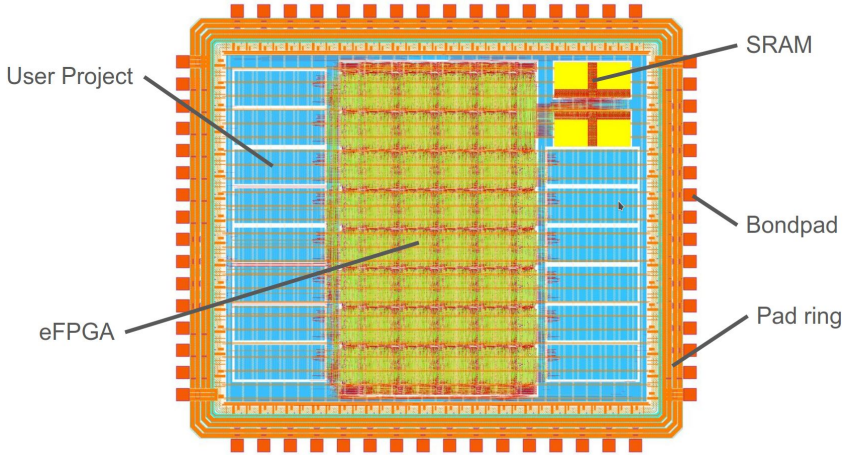
HEICHIPS 2025

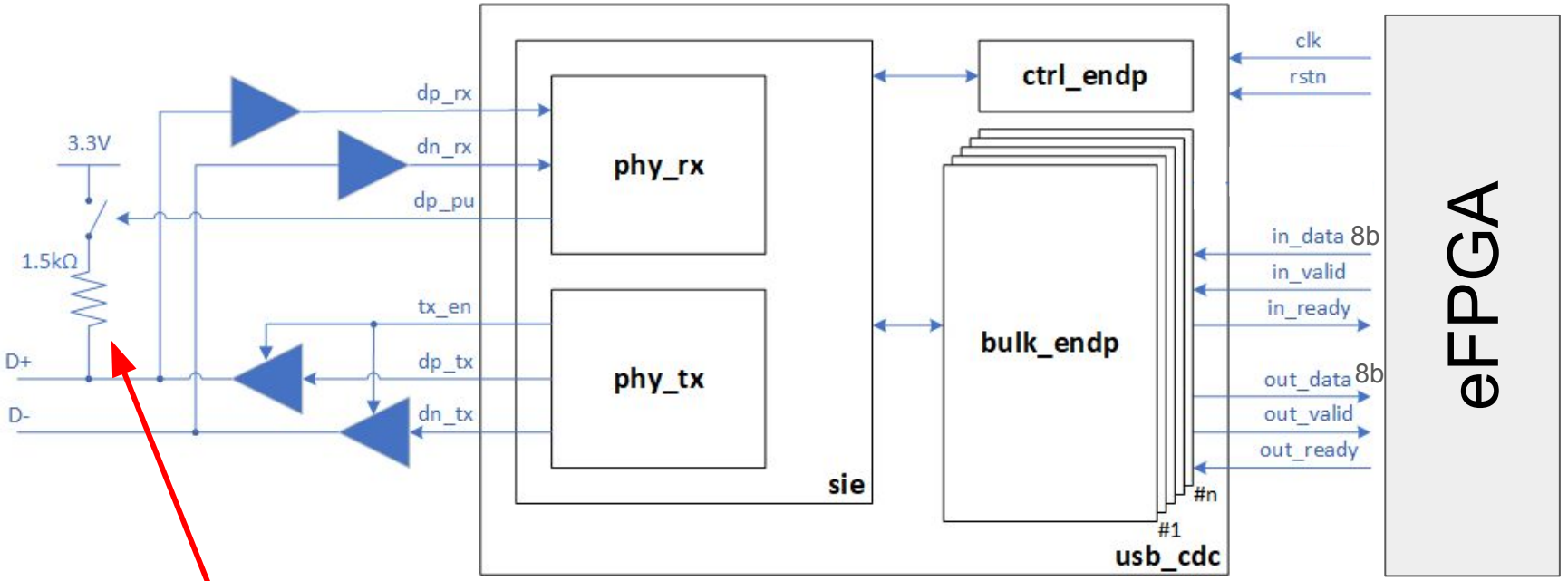
USB-CDC & spad_env_f_bit



Luis Ardila
Brian Pachideh
Francisco Sayas
Leo Moser

Project Repository

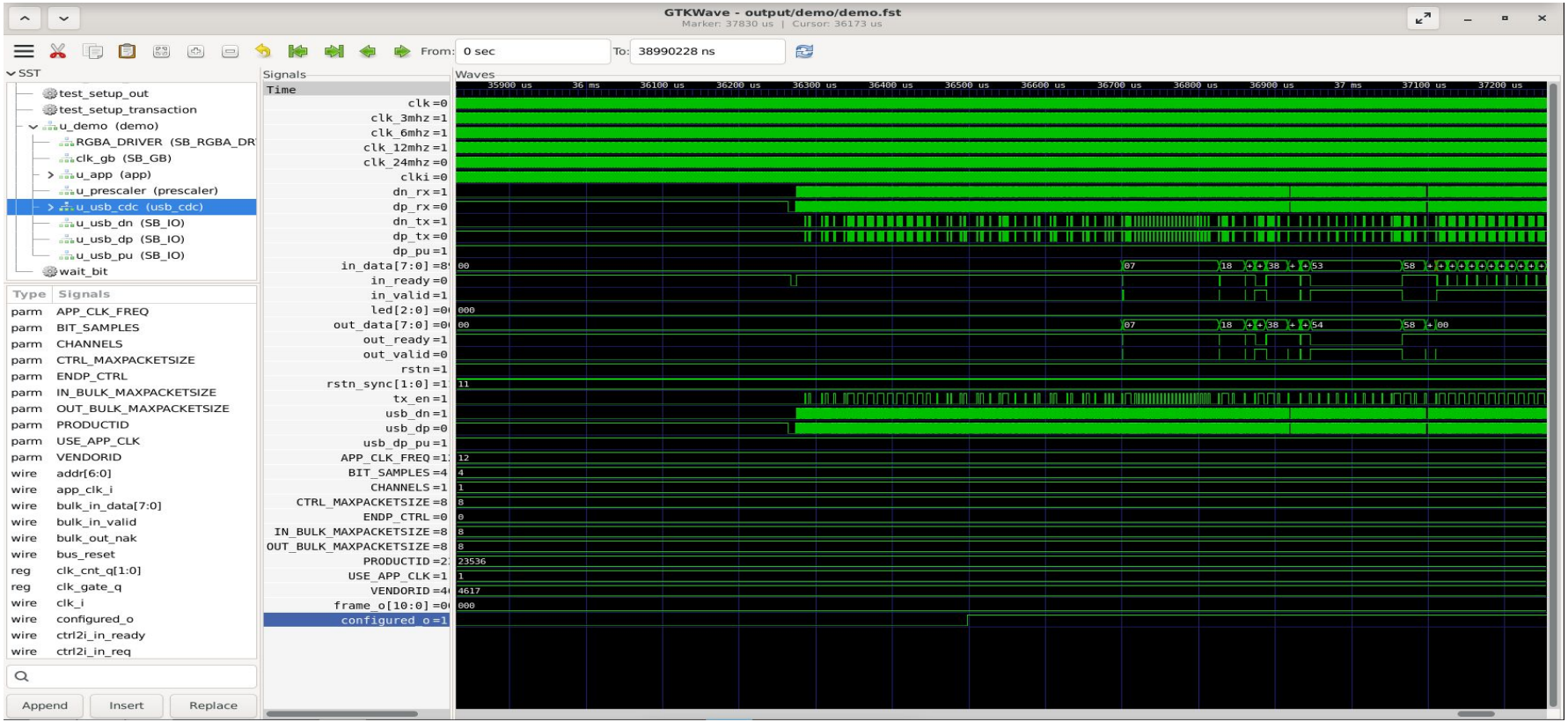
Architecture overview



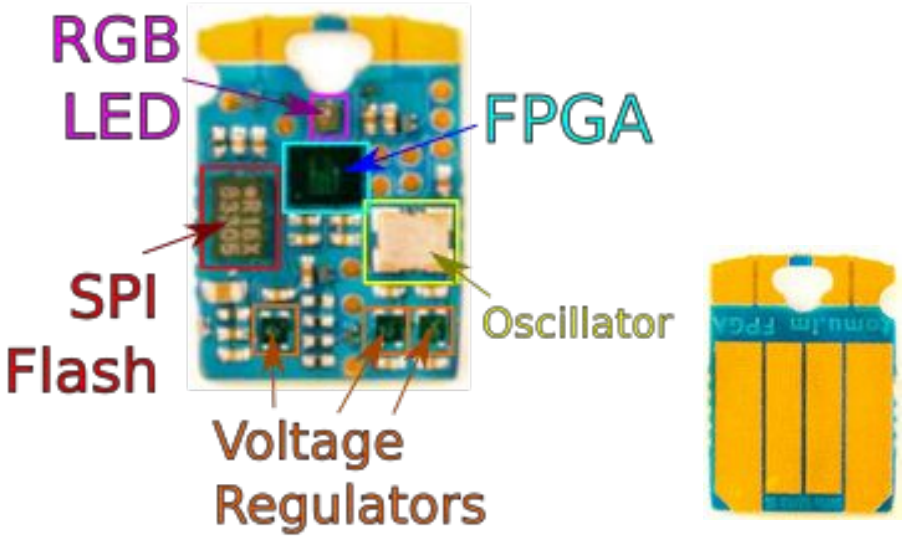
Resistor on PCB

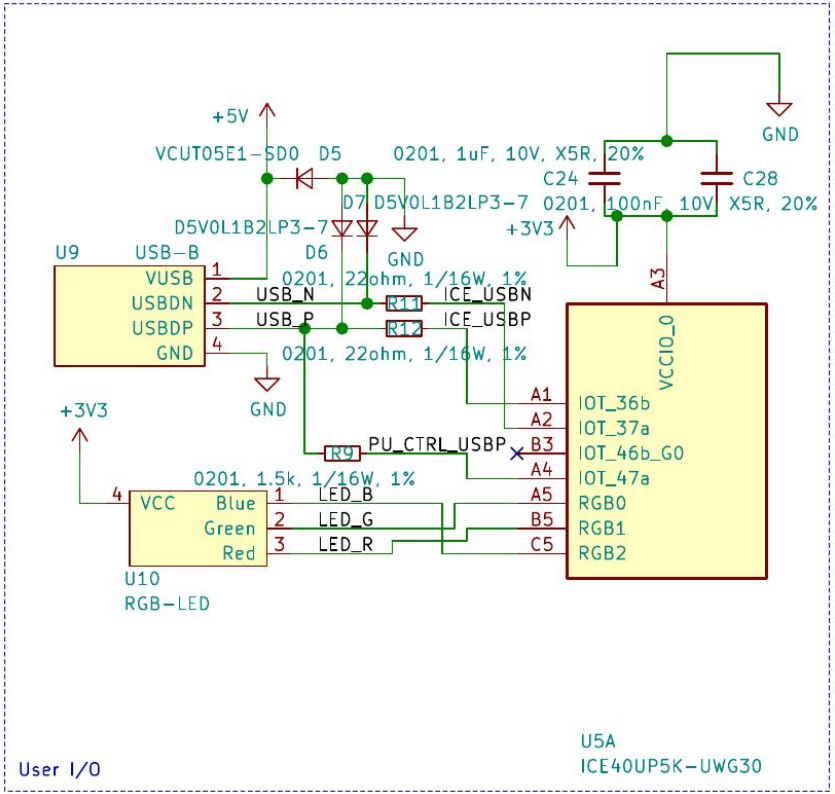
RTL from: https://github.com/ulixxe/usb_cdc
(USB 2.0 - Full Speed)

Verification on Simulation



Verification by doing FPGA emulation on Fomu





Direct FPGA pin to USB connector like [FOMU]

https://workshop.fomu.im/en/latest/index.html

Benchmark using Fomu and python utility

Max 443.2 kB/s

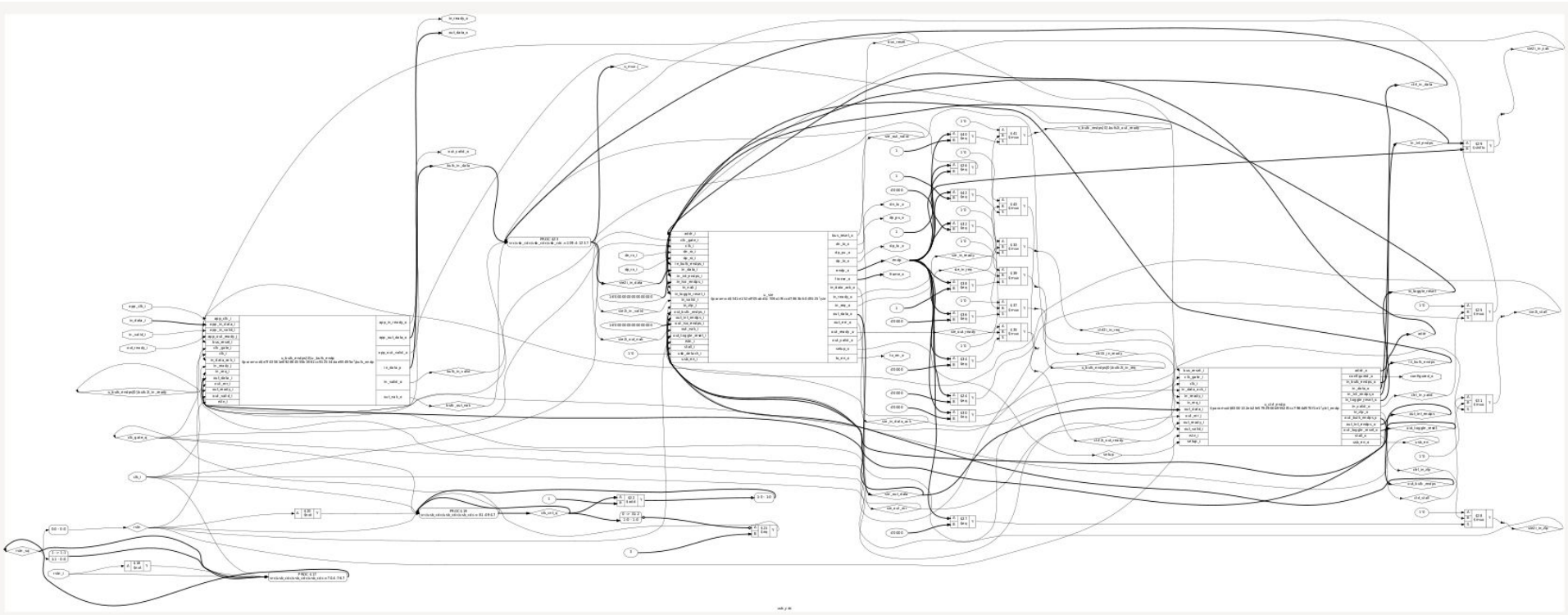
```
python3 run.py
LFSR = 0x0
OK! 4 bytes transferred in 0.0 sec (12.4 kB/s)
OK! 100000 bytes transferred in 0.226 sec (443.2 kB/s)
OK! 100000 bytes transferred in 0.243 sec (411.6 kB/s)
b'1111111111'
b'Hello World!Hello World!Hello World!Hello World!Hello World!Hello World!
0000: 72 6c 64 21 48 65 6c 6c 6f 20 57 6f 72 6c 64 21 | rld!Hello World!
0010: 48 65 6c 6c 6f 20 57 6f 72 6c 64 21 48 65 6c 6c | Hello World!Hell
0020: 6f 20 57 6f 72 6c 64 21 48 65 6c 6c 6f 20 57 6f | o World!Hello Wo
0030: 72 6c 64 21 48 65 6c 6c 6f 20 57 6f 72 6c 64 21 | rld!Hello World!
0040: 48 65 6c 6c 6f 20 57 6f 72 6c 64 21 48 65 6c 6c | Hello World!Hell
0050: 6f 20 57 6f 72 6c 64 21 48 65 6c 6c 6f 20 57 6f | o World!Hello Wo
0060: 72 6c 64 21 48 65 6c 6c 6f 20 57 6f 72 6c 64 21 | rld!Hello World!
0070: 48 65 6c 6c 6f 20 57 6f 72 6c 64 21 48 65 6c 6c | Hello World!Hell
```

```
0390: 72 6c 64 21 48 65 6c 6c 6f 20 57 6f 72 6c 64 21 | rld!Hello World!
03a0: 48 65 6c 6c 6f 20 57 6f 72 6c 64 21 48 65 6c 6c | Hello World!Hell
03b0: 6f 20 57 6f 72 6c 64 21 48 65 6c 6c 6f 20 57 6f | o World!Hello Wo
03c0: 72 6c 64 21 48 65 6c 6c 6f 20 57 6f 72 6c 64 21 | rld!Hello World!
03d0: 48 65 6c 6c 6f 20 57 6f 72 6c 64 21 48 65 6c 6c | Hello World!Hell
03e0: 6f 20 57 6f 72 6c 64 21 48 65 6c 6c 6f 20 57 6f | o World!Hello Wo
03f0: 72 6c 64 21 48 65 6c 6c 6f 20 57 6f 72 6c 64 21 | rld!Hello World!
0400: 72 6c 64 21                                     | rld!
OK! 1028 bytes transferred in 0.003 sec (338.3 kB/s)
b'6bff70f634535064f37b754c281f6af7b0a120a7ab23aa56c72b8196963ea96c42c6208931
OK! 1028 bytes transferred in 0.005 sec (224.6 kB/s)
```

Signal Reference

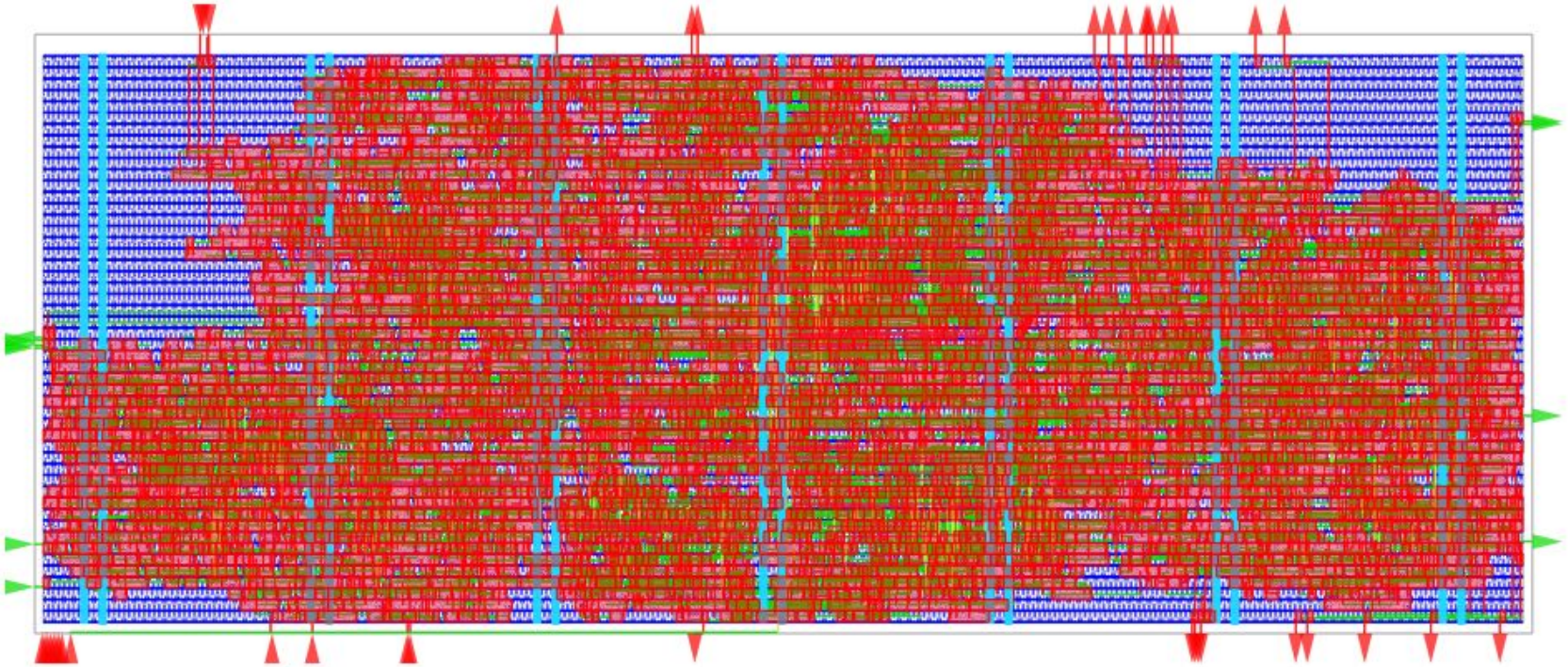
Heichips25 Template Signal	DIR	USB-CDC Signal	Notes
clk	I	clk_i	Clock 48MHz (single clock)
rst_n	I	rstn_i	Active-low reset
ena	I	unused	
ui_in[7:0]	I	in_data_i[7:0]	Data from eFPGA to USB core
uo_out[7:0]	O	out_data_o[7:0]	Data From USB core to eFPGA
~~uio_in[7:3]~~ uio_in[2] uio_in[1] uio_in[0]	I	~~unused~~ spad_hit_async out_ready_i in_valid_i	 Signal from the **spad_env_f_bit** core
uio_out[7] uio_out[6] uio_out[5] uio_out[4] uio_out[3] ~~uio_out[2:0]~~	O	env_bit configured_o in_ready_o out_valid_o env_valid ~~unused~~	Signal from the **spad_env_f_bit** core Signal from the **spad_env_f_bit** core
uio_en[7:0]	O	0xF0	Bidirectional bus output enable fixed value with (4 outputs and 4 inputs)
usb_dp_en_o	O	tx_en_o	USB D+ enable (to output buff)
usb_dp_rx_i	I	dp_rx_i	USB D+ receive (from pad)
usb_dp_tx_o	O	dp_tx_o	USB D+ transmit (to pad)
usb_dn_en_o	O	tx_en_o	USB D- enable (to output buff)
usb_dn_rx_i	I	dn_rx_i	USB D- receive (from pad)
usb_dn_tx_o	O	dn_tx_o	USB D- transmit (to pad)
usb_dp_up_o	O	dp_up_o	USB D+ pull-up to external 1.5k res

Architecture view after running synthesis using yosys



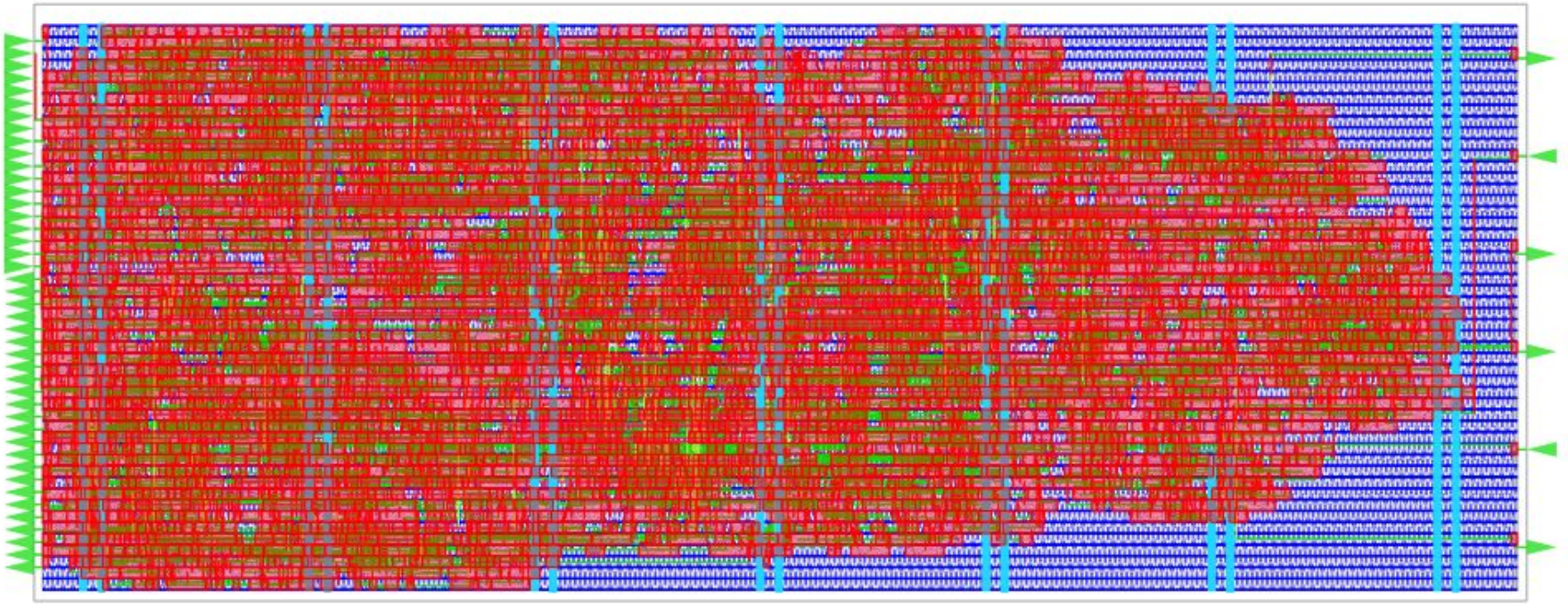
Layout without template

Default template did not work since there are extra pins declared



Layout with custom USB template

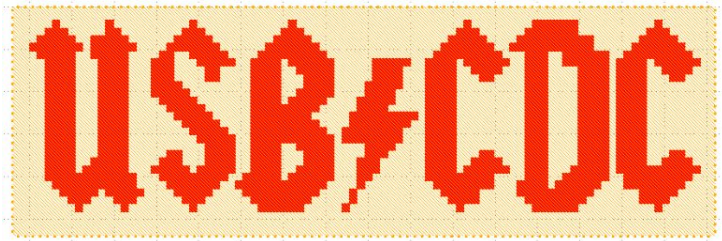
Dedicated USB pins located on the right



Logo in GDS

using greyhound script
to convert input PNG

DRC clean!



eFPGA demo

Full “Hello world” example to connect with your designs

Sends “Hello World” characters

Simple fabric interface:

- in_data[7:0]
- In_valid, in_ready
- out_data[7:0]
- out_valid, out_ready

```
        hello_world[5]  = " ";
        hello_world[6]  = "W";
        hello_world[7]  = "o";
        hello_world[8]  = "r";
        hello_world[9]  = "l";
        hello_world[10] = "d";
    end

always @(posedge clk) begin
    if (!rst_n) begin
        // Reset all stateful elements
        counter          <= 0;
        byte_index       <= 0;
        send_enable      <= 0;
        usb_in_data_reg  <= 0;
        usb_in_valid_reg <= 0;
    end else begin
        counter <= counter + 1;

        if (counter >= 24'd12_000_000) begin
            counter     <= 0;
            byte_index  <= 0;
            send_enable <= 1;
        end

        if (send_enable && usb_in_ready) begin
            usb_in_data_reg  <= hello_world[byte_index];
            usb_in_valid_reg <= 1;
            byte_index       <= byte_index + 1;
```

WIP - cocotb testbench

```
FST info: dumpfile /home/user/work/heichips25-usb_cdc/tb/sim_build/heichips25_usb_cdc.fst opened for outp
100200.00ns INFO     cocotb                          Starting USB CDC loopback test
103520.00ns INFO     cocotb                          ✓ SOF test passed
113603.00ns INFO     cocotb                          ✓ USB reset test passed
113603.00ns INFO     cocotb                          Testing loopback with 7 bytes
124698.00ns WARNING  cocotb                          OUT transfer response: 10
129780.00ns WARNING  cocotb                          IN transfer timeout - no device response
129780.00ns INFO     cocotb                          ✓ Loopback test 1 completed
130780.00ns INFO     cocotb                          Testing loopback with 8 bytes
142548.00ns WARNING  cocotb                          OUT transfer response: 10
147630.00ns WARNING  cocotb                          IN transfer timeout - no device response
147630.00ns INFO     cocotb                          ✓ Loopback test 2 completed
148630.00ns INFO     cocotb                          Testing loopback with 4 bytes
157731.00ns WARNING  cocotb                          OUT transfer response: 10
162813.00ns WARNING  cocotb                          IN transfer timeout - no device response
162813.00ns INFO     cocotb                          ✓ Loopback test 3 completed
172113.00ns INFO     cocotb                          ✅ USB CDC loopback test completed successfully!
172113.00ns INFO     cocotb.regression               usb_cdc_loopback_test passed
```

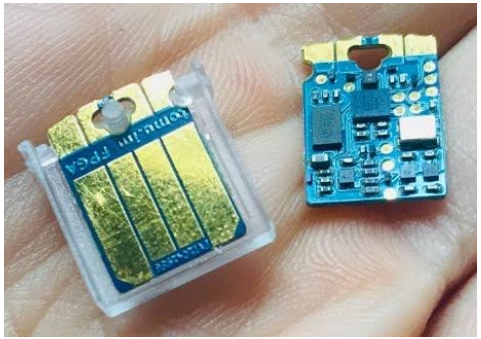
Overall milestones achievements

- **Physical verification** made on Fomu FPGA board
- **ASIC implementation** fits into small project tile (500x200)
  - USB IP requires global clock of 48MHz
- **Logo** implemented in Topmetal 1 added by script as part of the final macro copy step
- **spad_env_f_bit** project included as hardened macro

WIP:

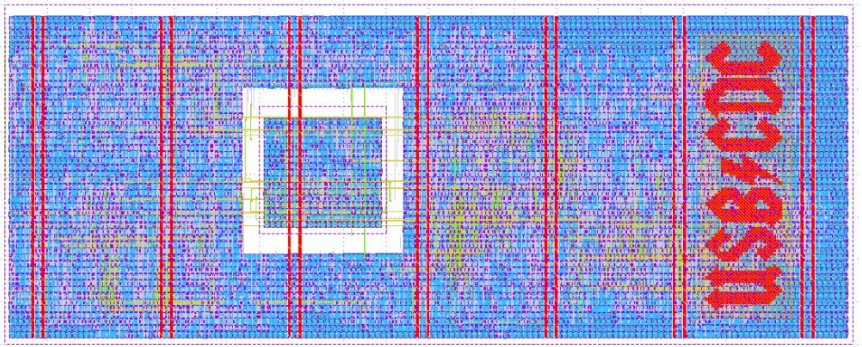
- Example **eFabric design for integration** with other projects/modules
- Porting of loopback testbench to cocotb template for **behav + gate level sim**

[Project Repository]



Fomu FPGA Board

Final GDS



Certain layers were turned off to increase logo visibility