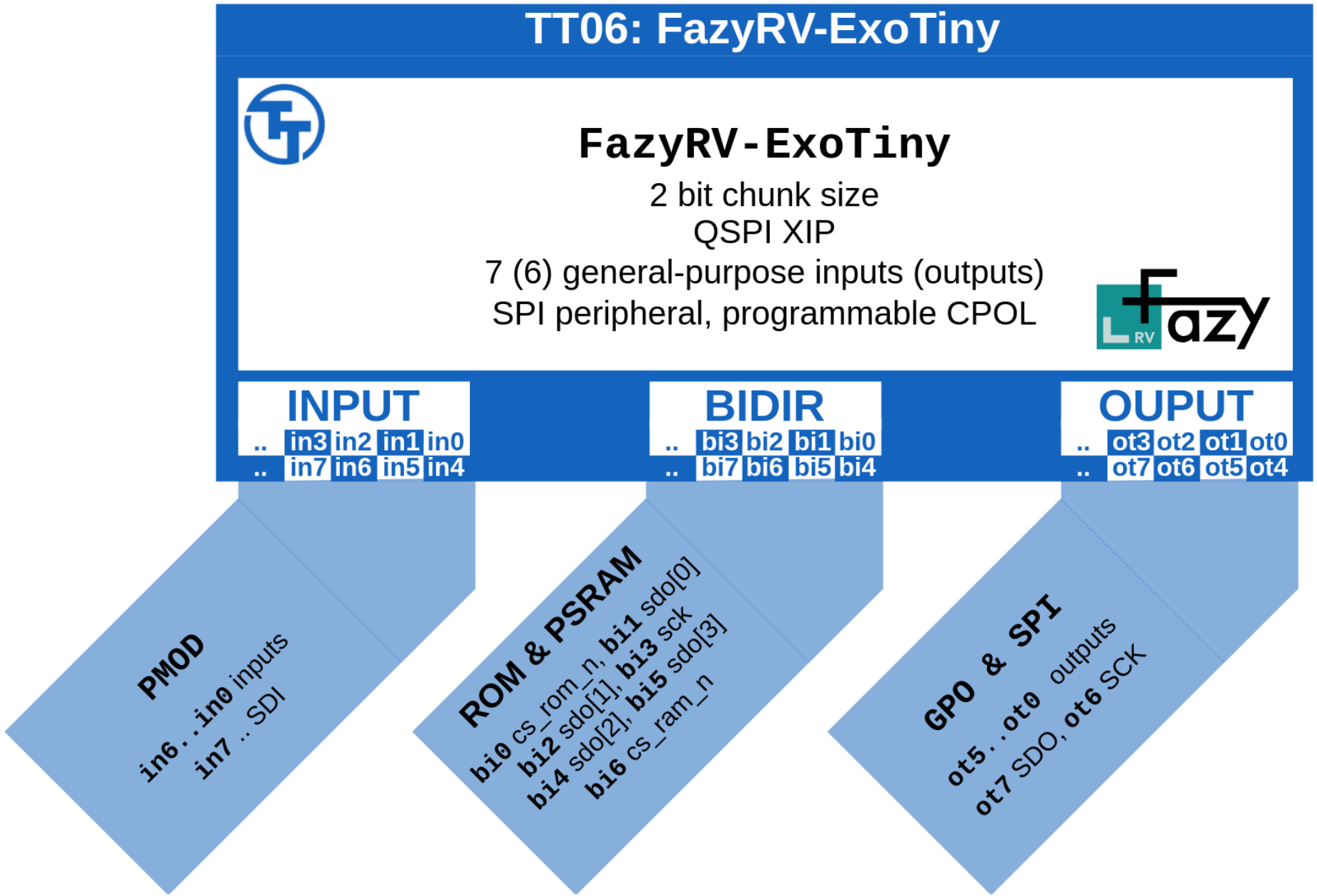
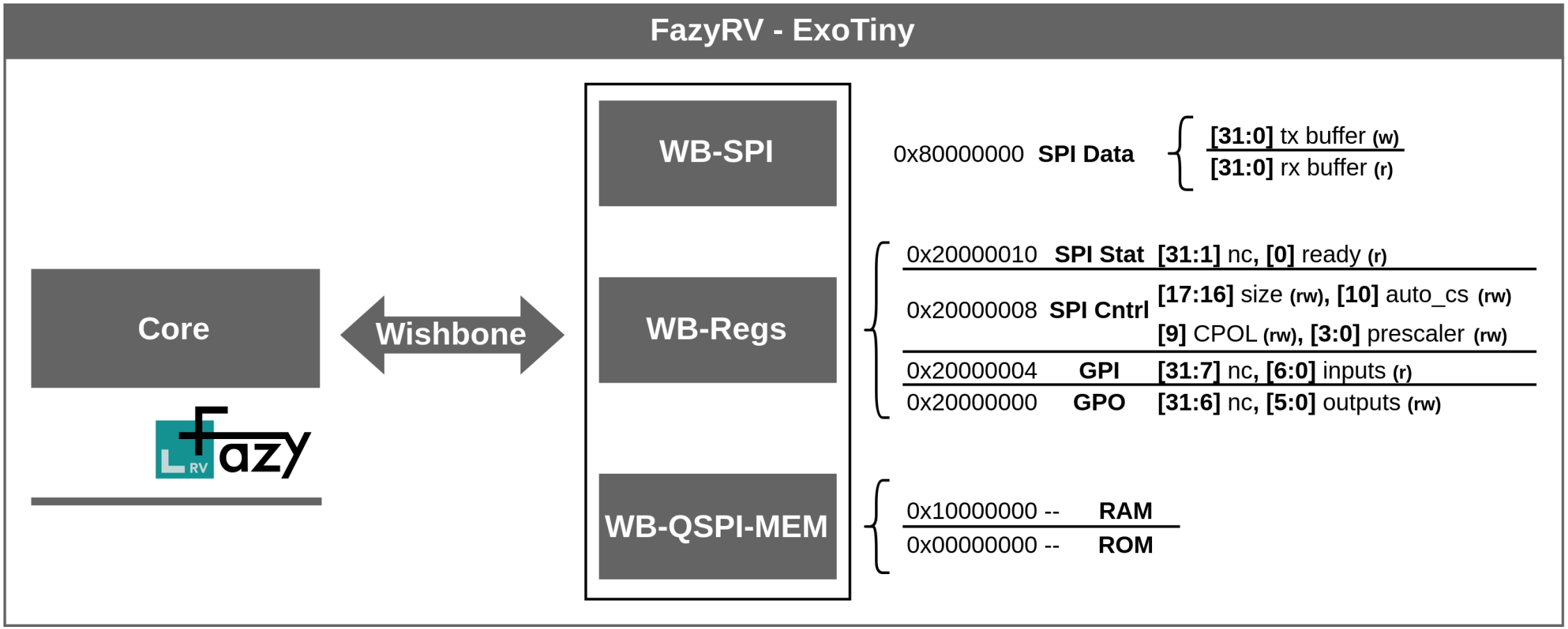
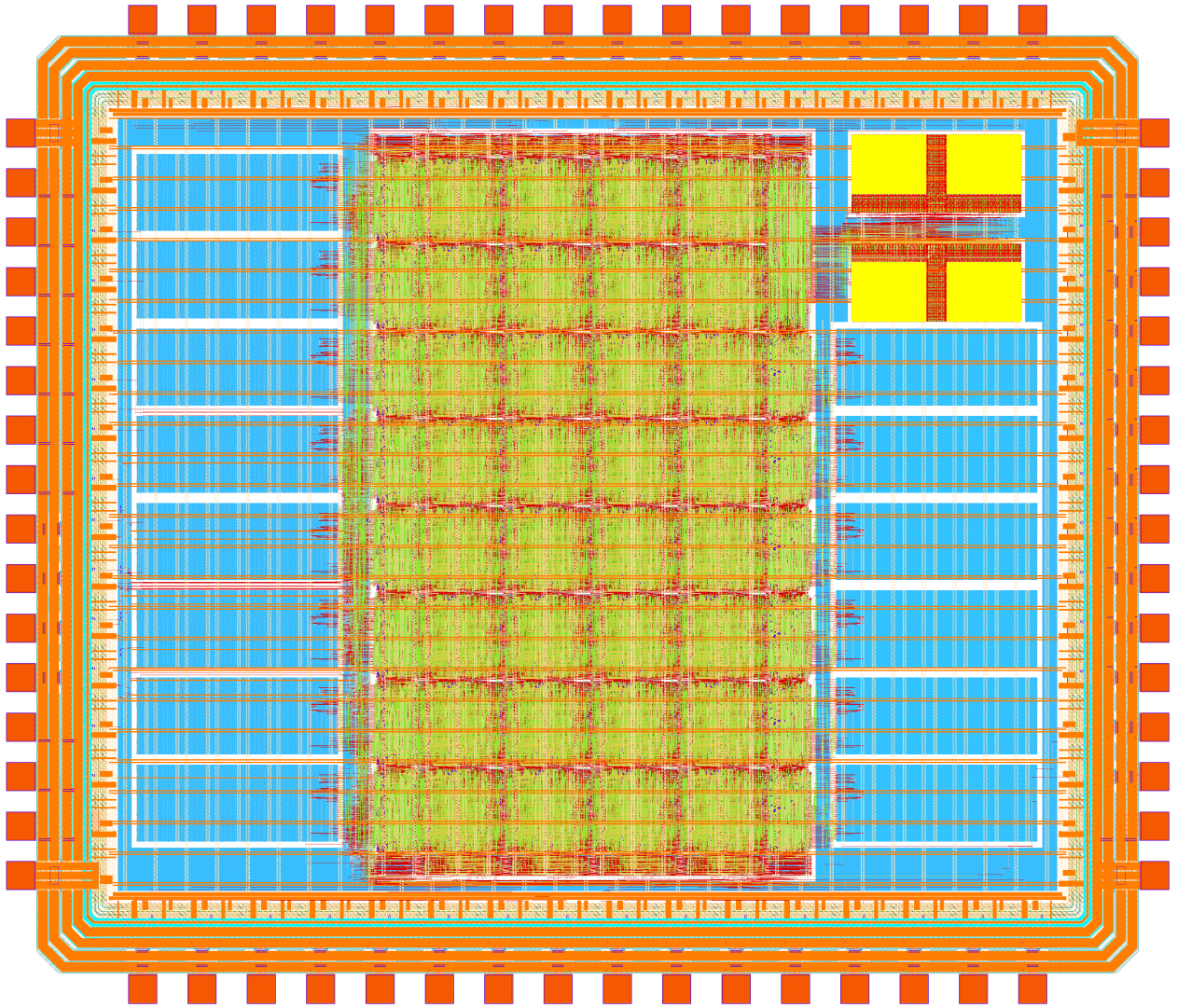
FazyRV-ExoTiny CCX

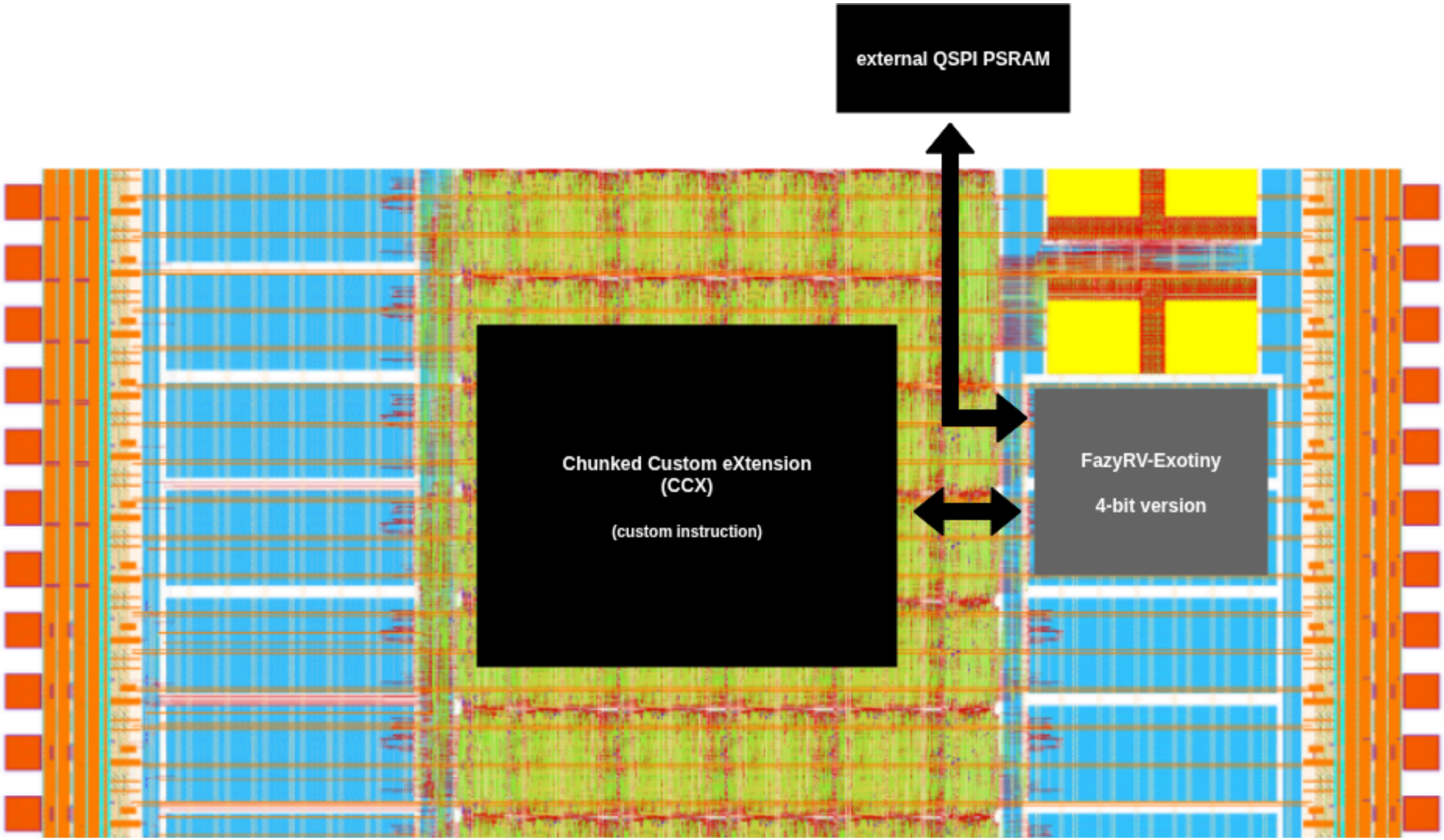
HeiChips'25

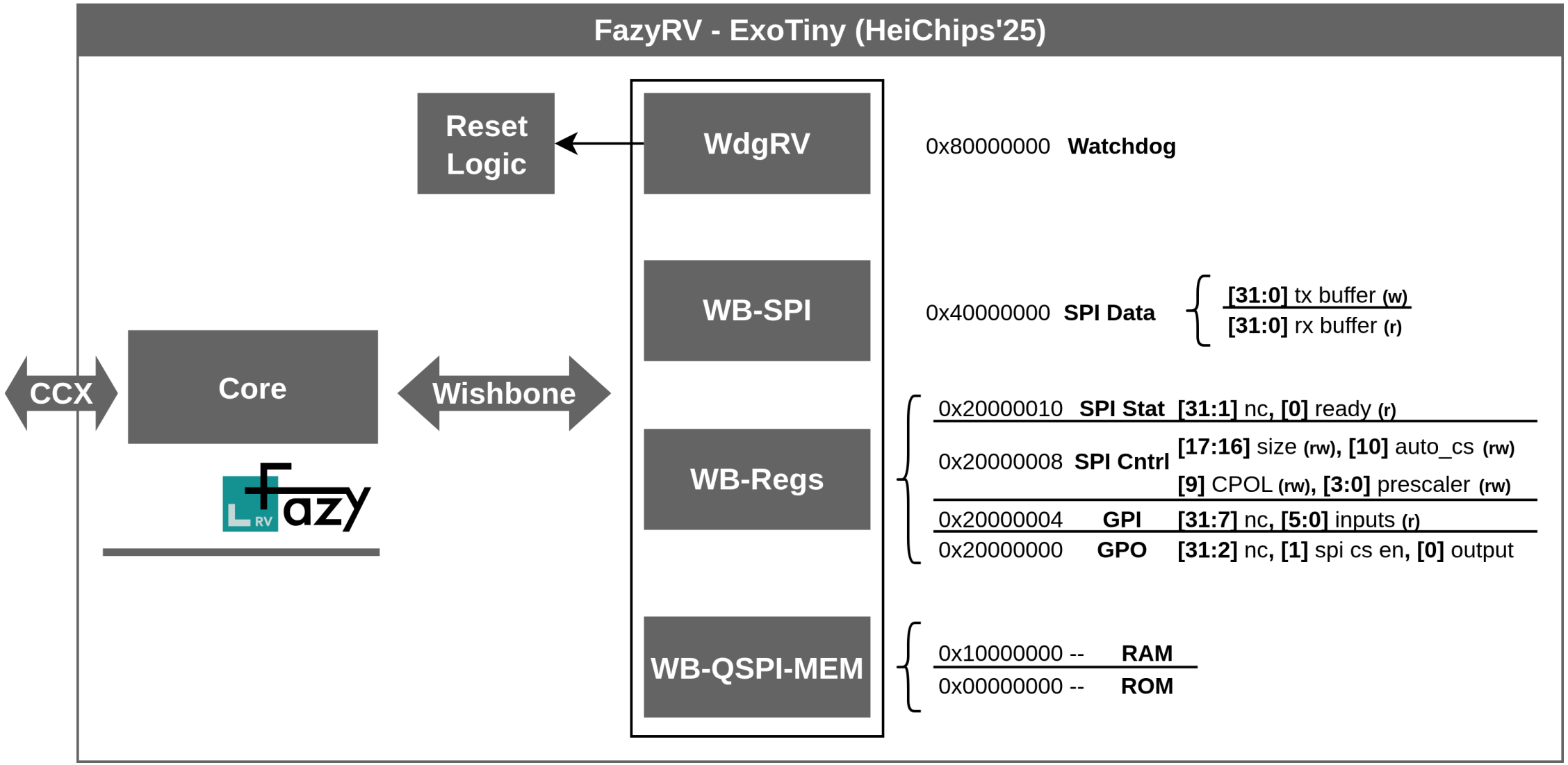
Spandan Das
Meinhard Kissich (@meiniKi)
Marcin Kowalczyk (@MPKowalczyk)
Matthias Musch (@matztron)
Muhammad Sabih


TT06: FazyRV-ExoTiny
FazyRV-ExoTiny
2 bit chunk size
QSPI XIP
7 (6) general-purpose inputs (outputs)
SPI peripheral, programmable CPOL
INPUT
.. in3 in2 in1 in0
.. in7 in6 in5 in4
BIDIR
.. bi3 bi2 bi1 bi0
.. bi7 bi6 bi5 bi4
OUPUT
.. ot3 ot2 ot1 ot0
.. ot7 ot6 ot5 ot4
PMOD
in6..in0 inputs
in7 .. SDI
ROM & PSRAM
bi0 cs_rom_n, bi1 sdo[0]
bi2 sdo[1], bi3 sck
bi4 sdo[2], bi5 sdo[3]
bi6 cs_ram_n
GPO & SPI
ot5..ot0 outputs
ot7 SDO, ot6 SCK

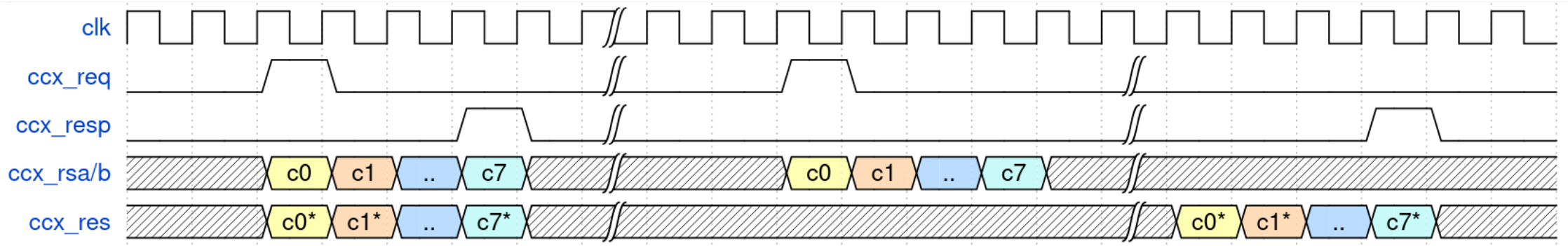

FazyRV - ExoTiny
Core
Wishbone
WB-SPI
WB-Regs
WB-QSPI-MEM
0x80000000 SPI Data
[31:0] tx buffer (w)
[31:0] rx buffer (r)
0x20000010 SPI Stat [31:1] nc, [0] ready (r)
0x20000008 SPI Cntrl [17:16] size (rw), [10] auto_cs (rw)
[9] CPOL (rw), [3:0] prescaler (rw)
0x20000004 GPI [31:7] nc, [6:0] inputs (r)
0x20000000 GPO [31:6] nc, [5:0] outputs (rw)
0x10000000 -- RAM
0x00000000 -- ROM




external QSPI PSRAM
Chunked Custom eXtension
(CCX)
(custom instruction)
FazyRV-Exotiny
4-bit version


FazyRV - ExoTiny (HeiChips'25)
Reset Logic
WdgRV
0x80000000 Watchdog
WB-SPI
0x40000000 SPI Data
[31:0] tx buffer (w)
[31:0] rx buffer (r)
CCX
Core
Wishbone
WB-Regs
0x20000010 SPI Stat [31:1] nc, [0] ready (r)
0x20000008 SPI Cntrl [17:16] size (rw), [10] auto_cs (rw)
[9] CPOL (rw), [3:0] prescaler (rw)
0x20000004 GPI [31:7] nc, [5:0] inputs (r)
0x20000000 GPO [31:2] nc, [1] spi cs en, [0] output
WB-QSPI-MEM
0x10000000 -- RAM
0x00000000 -- ROM

CCX Interface

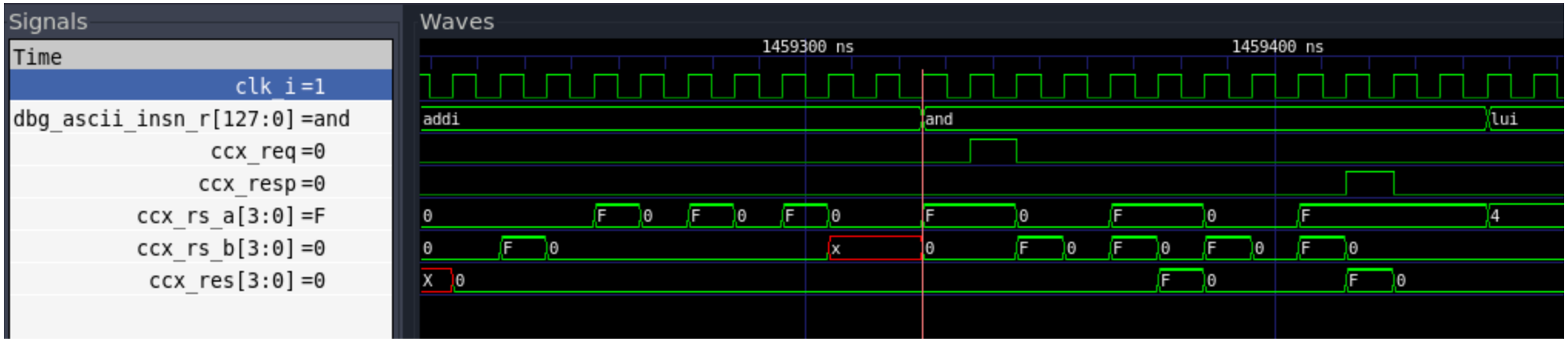


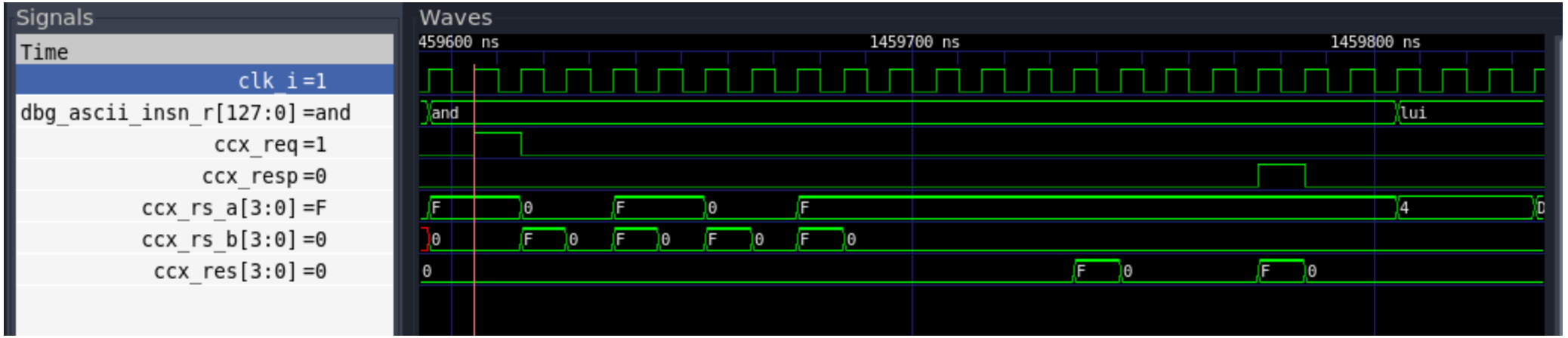
Smoke Test

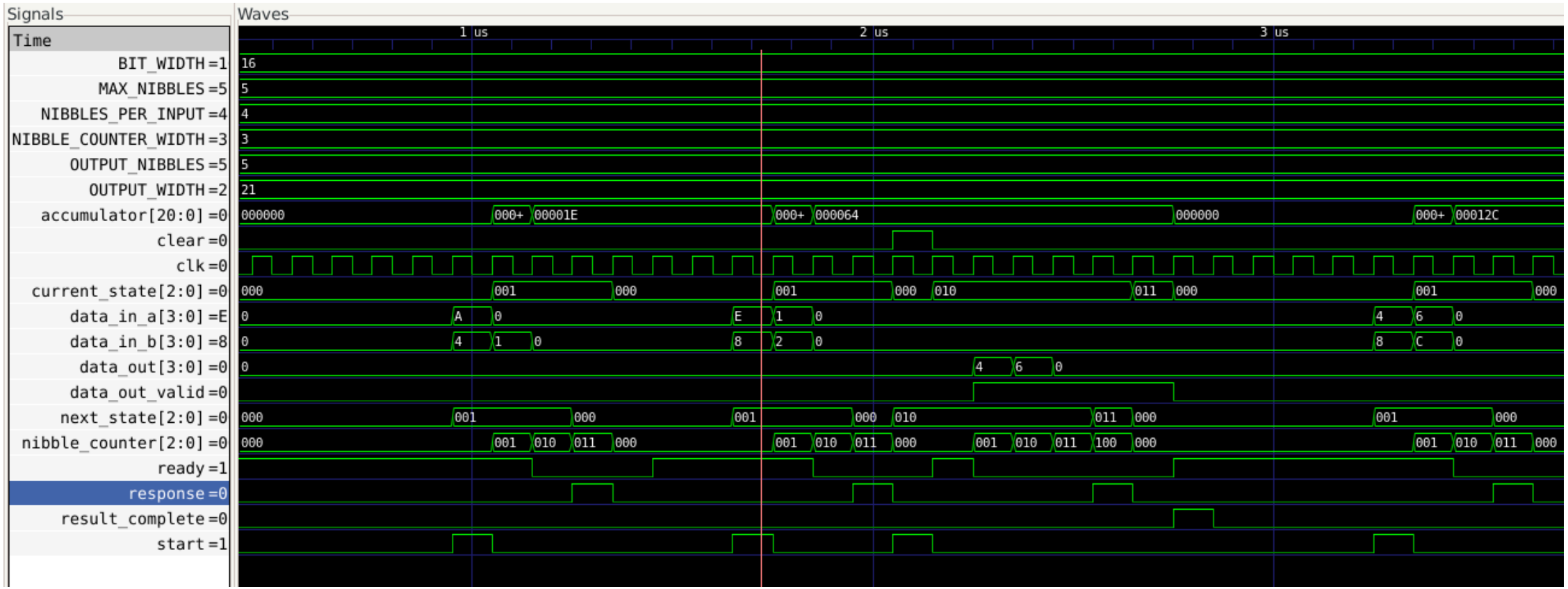
- Implement an `AND` as CCX
- Modify the decoder

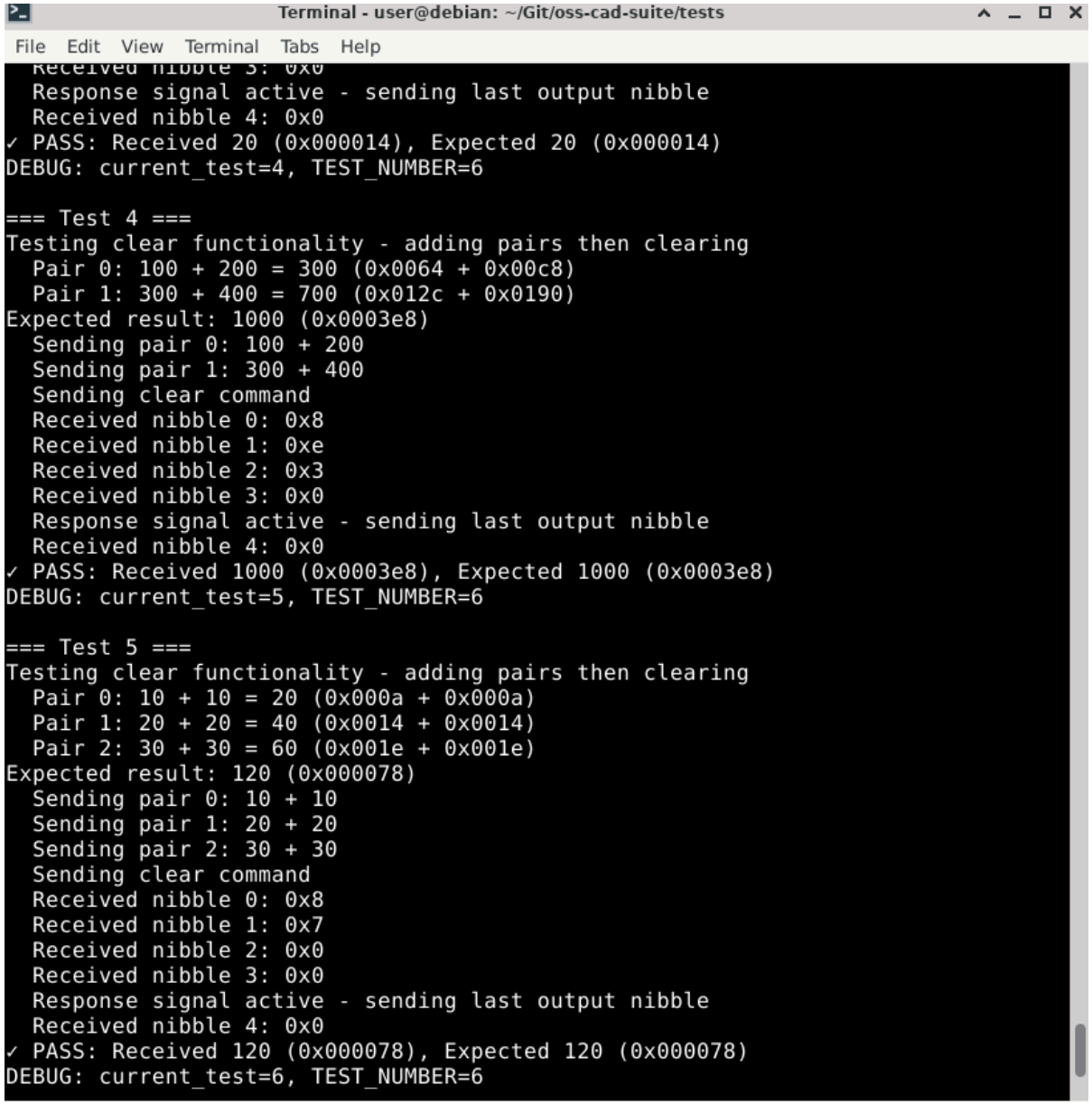
```
always_comb begin
  if ((instr_i[6:0] == 'b0110011) && (instr_i[14:12] == 'h7)) begin
    instr = {instr_i[21:15], 3'b0, instr_i[11:7], 7'h5B};
  end else begin
    instr = instr_i;
  end
```

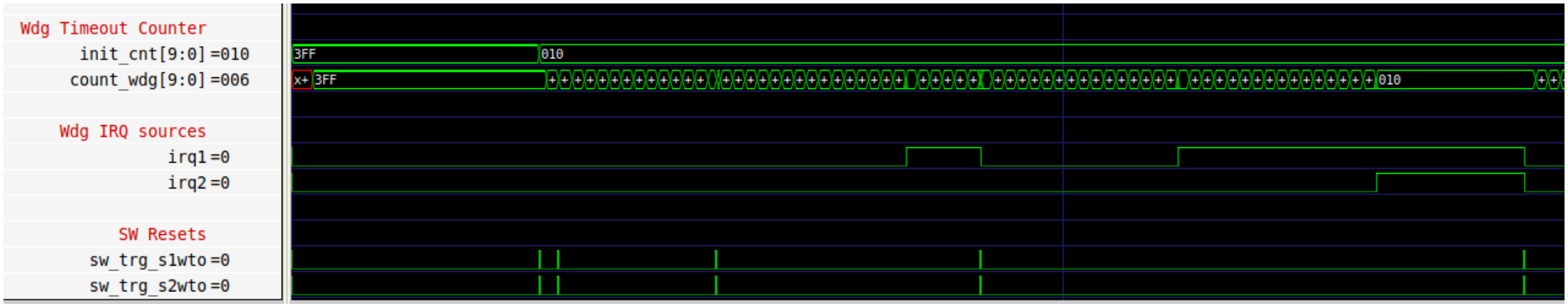
- Run riscv-tests

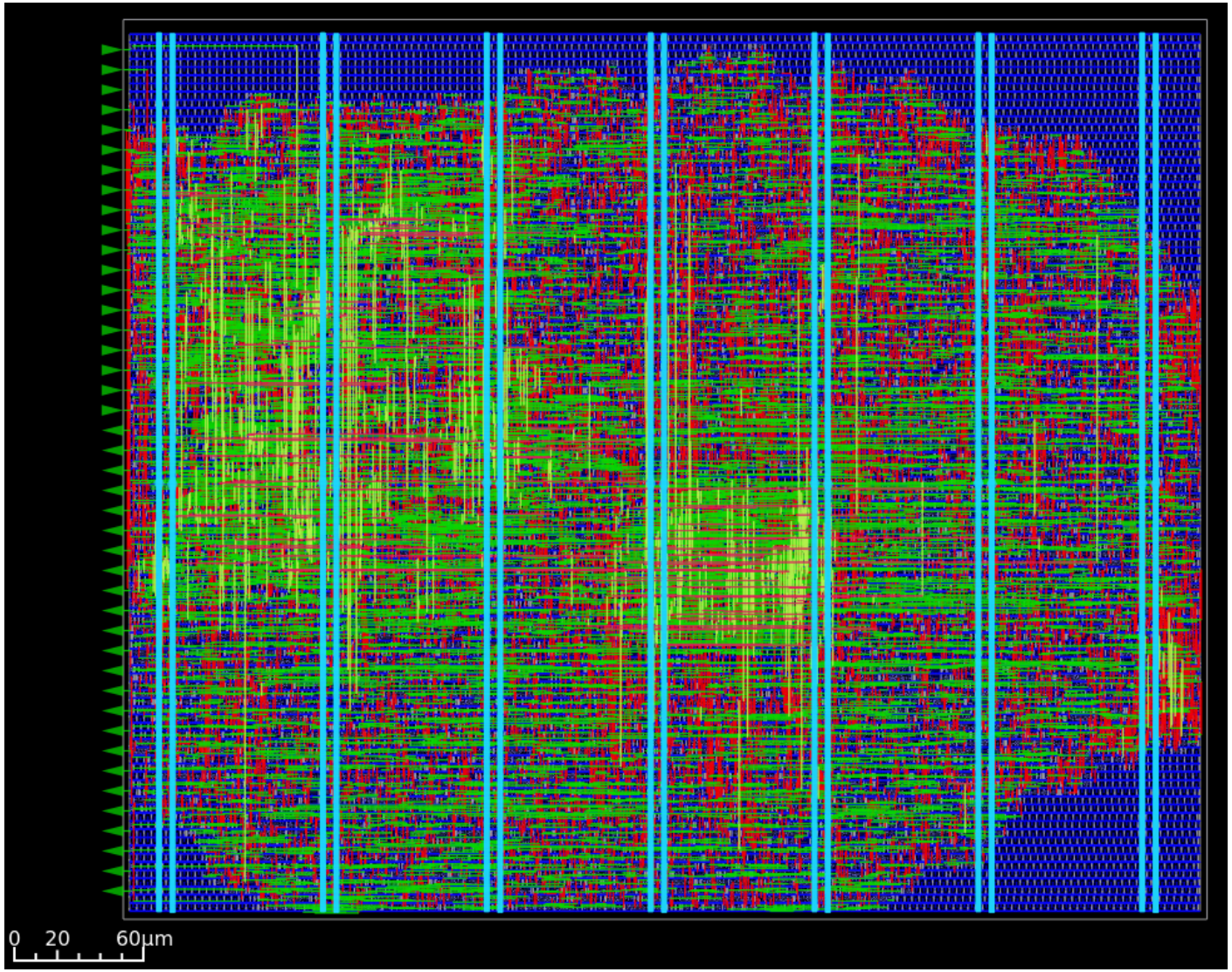

Signals
Waves
Time
clk_i=1
dbg_ascii_insn_r[127:0]=and
ccx_req=0
ccx_resp=0
ccx_rs_a[3:0]=F
ccx_rs_b[3:0]=0
ccx_res[3:0]=0
1459300 ns
1459400 ns
addi
and
lui


Signals
Waves
Time
clk_i=1
dbg_ascii_insn_r[127:0]=and
ccx_req=1
ccx_resp=0
ccx_rs_a[3:0]=F
ccx_rs_b[3:0]=0
ccx_res[3:0]=0
459600 ns
1459700 ns
1459800 ns
and
lui


Signals
Waves
Time
BIT_WIDTH =1
MAX_NIBBLES =5
NIBBLES_PER_INPUT =4
NIBBLE_COUNTER_WIDTH =3
OUTPUT_NIBBLES =5
OUTPUT_WIDTH =2
accumulator[20:0] =0
clear =0
clk =0
current_state[2:0] =0
data_in_a[3:0] =E
data_in_b[3:0] =8
data_out[3:0] =0
data_out_valid =0
next_state[2:0] =0
nibble_counter[2:0] =0
ready =1
response =0
result_complete =0
start =1
1 us
2 us
3 us


Terminal - user@debian: ~/Git/oss-cad-suite/tests
File Edit View Terminal Tabs Help
  Received nibble 3: 0x0
  Response signal active - sending last output nibble
  Received nibble 4: 0x0
✓ PASS: Received 20 (0x000014), Expected 20 (0x000014)
DEBUG: current_test=4, TEST_NUMBER=6
=== Test 4 ===
Testing clear functionality - adding pairs then clearing
  Pair 0: 100 + 200 = 300 (0x0064 + 0x00c8)
  Pair 1: 300 + 400 = 700 (0x012c + 0x0190)
Expected result: 1000 (0x0003e8)
  Sending pair 0: 100 + 200
  Sending pair 1: 300 + 400
  Sending clear command
  Received nibble 0: 0x8
  Received nibble 1: 0xe
  Received nibble 2: 0x3
  Received nibble 3: 0x0
  Response signal active - sending last output nibble
  Received nibble 4: 0x0
✓ PASS: Received 1000 (0x0003e8), Expected 1000 (0x0003e8)
DEBUG: current_test=5, TEST_NUMBER=6
=== Test 5 ===
Testing clear functionality - adding pairs then clearing
  Pair 0: 10 + 10 = 20 (0x000a + 0x000a)
  Pair 1: 20 + 20 = 40 (0x0014 + 0x0014)
  Pair 2: 30 + 30 = 60 (0x001e + 0x001e)
Expected result: 120 (0x000078)
  Sending pair 0: 10 + 10
  Sending pair 1: 20 + 20
  Sending pair 2: 30 + 30
  Sending clear command
  Received nibble 0: 0x8
  Received nibble 1: 0x7
  Received nibble 2: 0x0
  Received nibble 3: 0x0
  Response signal active - sending last output nibble
  Received nibble 4: 0x0
✓ PASS: Received 120 (0x000078), Expected 120 (0x000078)
DEBUG: current_test=6, TEST_NUMBER=6


Wdg Timeout Counter
init_cnt[9:0]=010
count_wdg[9:0]=006
Wdg IRQ sources
irq1=0
irq2=0
SW Resets
sw_trg_s1wto=0
sw_trg_s2wto=0
3FF
010
x+
3FF
010



preliminary implementation

Physical Implementation

- https://github.com/meiniKi/heichips25-fazyrv-exotiny

FazyRV ExoTiny SoC

- https://github.com/meiniKi/fazyrv-exotiny

FazyRV RISC-V Core

- https://github.com/meiniKi/fazyrv

Watchdog

- https://github.com/matztron/WdgRV

TT06 SoC

- https://github.com/meiniKi/tt06-FazyRV-ExoTiny