A Highly Linear Wide Bandwidth Programmable Gain Amplifier in $0.18\mu m$ CMOS Process

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Introduction

Variable Gain Amplifiers (VGAs) and Programmable Gain Amplifiers (PGAs) are vital in applications such as medical electronic devices, telecommunications, and disk drives, where dynamic range and signal fidelity are critical.

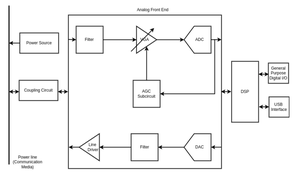


Figure 1. A generic wireline communication transceiver showing an analog frontend with a VGA in AGC loop. Adapted from [4].

Problem Statement

Modern communication and signal processing systems require PGAs that not only provide a high dB-in-linear gain range but also maintain wide bandwidth, high slew rate, low power consumption, low noise, and compact chip area. Meeting all these requirements simultaneously remains a design challenge.

Motivation

This work is inspired by the 2023 IEEE SSCS Lab-Bench-on-a-Chip open-source chipathon initiative, where the PGA is a critical component of the signal conditioning block. Achieving a high-performance PGA is essential to meeting the overall system-level requirements.

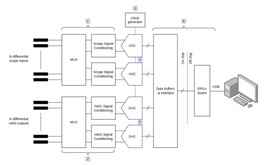


Figure 2. Lab-bench on a chip project with analog and digital sub-block. Adapted from the IEEE SSCS Chipathon webpage [1].

Project Goal and Design Approach

This project aims to develop a CMOS PGA that achieves high linearity, wide bandwidth, low power consumption, and a wide programmable gain range — suitable for integration into modern signal processing systems.

Design Approach The proposed architecture uses an Operational Transconductance Amplifier (OTA) with series and feedback switch-resistor networks to enhance linearity and allow programmable gain control. The target specifications include: Gain range: −12 dB to 20 dB, Bandwidth: 100–500 MHz Distortion: ≤ −55 dB, Power consumption: ≤ 25 mW. The design is implemented using the open-source 0.18 µm CMOS process (GF180) from GlobalFoundries.

Aim and Objectives

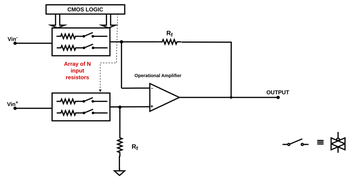
Aim: Implement a programmable gain amplifier (PGA) optimized for high linearity, bandwidth, and energy efficiency in CMOS technology.

Aim and Objectives

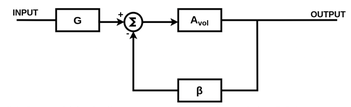
Specific objectives include:

- Develop a suitable amplifier topology for the PGA core.
- Integrate switch-resistor feedback to achieve linear dB-in-gain control
- Design supporting bias/reference circuits and the transmission gate switches
- Implement and tape out using the 0.18µm GlobalFoundries CMOS process

Methodology



(a) The amplifier with series and feedback resistive network



(b) Control block diagram representation of the PGA architecture

Figure 3. Conceptual block diagram of the PGA. Adapted from [3].

$$A_{cl} = -\frac{G \cdot A_{vol}}{1 + \beta \cdot A_{vol}} \tag{1}$$

If $\beta \cdot A_{vol} >> 1$, then: $A_{cl} = -\frac{G}{\beta}$

But: $G = \frac{R_f}{R_f + R_i}$ and $\beta = \frac{R_i}{R_f + R_i}$

$$A_{cl} = -\frac{R_f}{R_i} \tag{2}$$

Where:

A_{cl} is the closed-loop gain, A_{vol} is the open-loop gain

β is the feedback factor, G is part of the feed forward gain

A_{cl} is the closed-loop gain, R_f and R_i are the feedback and series resistors, respectively.

The topologies of the core amplifier

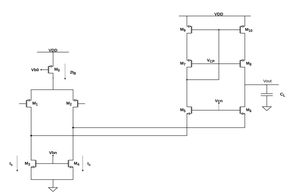


Figure 4. The conventional folded cascode topology. Adapted from [2].

Methodology Continued

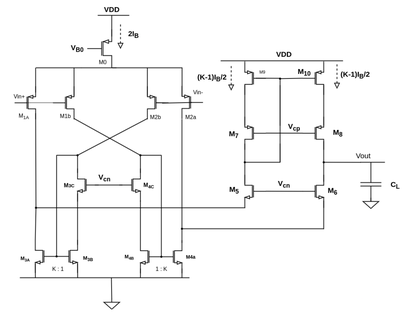


Figure 5. The recycling folded cascode topology. Adapted from [2].

Why Recycling folded cascode?

- More transconductance G_m; about 2× more
- About 2× more gain bandwidth (GBW) product
- About 3× slew rate (SR); faster settling time
- About 7-10 dB additional gain
- Better performance for same power consumption

$$G_{m,RFC} = g_{m1A} \cdot (1 + K) \tag{3}$$

$$GBW_{FC} = \frac{G_{m,FC}}{2\pi \cdot C_L} = \frac{g_m1}{2\pi \cdot C_L} \tag{4}$$

$$GBW_{RFC} = \frac{G_{m,RFC}}{2\pi \cdot C_L} = \frac{g_{m1A}(1 + K)}{2\pi \cdot C_L} \tag{5}$$

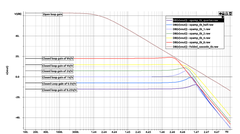
$$A_{v,FC} = g_{m1} \cdot g_{m6} r_{o6} (\frac{r_{o2A} || r_{o4A}}{2}) || g_{m8} r_{o8} r_{o10} \tag{6}$$

$$A_{v,RFC} = g_{m1A}(1 + K) \cdot g_{m6} r_{o6} (r_{o2A} || r_{o4A}) || g_{m8} r_{o8} r_{o10} \tag{7}$$

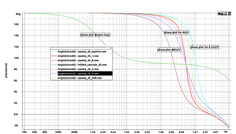
$$SR_{FC} = \frac{2 \cdot I_B}{C_L} \tag{8}$$

$$SR_{RFC} = \frac{2K \cdot I_B}{C_L} \tag{9}$$

Simulation Results



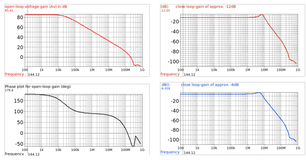
(a) Magnitude plot showing the open-loop gain and the closed-loop gains of the conventional folded-cascode-based PGA



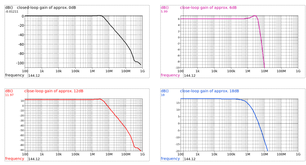
(b) The phase plot of the open-loop gain and the closed loop gains of the conventional folded-cascode-based PGA

Figure 6. Frequency response results of the PGA using conventional FC topology

Simulation Results Continued



(a) (i) Open-loop magnitude plot of the RFC OTA (ii) Closed-loop magnitude plot for gain 0.25V/V (iii) Open-loop phase plot of the OTA (iv) Closed-loop magnitude plot for gain 0.5V/V



(b) (v) Magnitude plot for gain 1V/V (vi) Magnitude plot for gain 2V/V (vii) Magnitude plot for gain 4V/V (viii) Magnitude plot for gain 8V/V

Figure 7. Frequency response results of the PGA using RFC topology

Conclusion and Future Work

The core amplifier topology of the PGA has been implemented using both a conventional folded cascode (FC) and a recycling folded cascode (RFC). The RFC improved open-loop gain — critical for accurate closed-loop gain ratio. The core amplifier achieved a figure of merit (FOM) of 1187MHzpF/mA. Feedback helped extend the closed-loop bandwidth by a factor of 100. However,the closed-loop bandwidth is approximately at 1-2 MHz, still below the target bandwidth.

Future Work: To achieve the target closed-loop bandwidth of 100-500 MHz, current operational amplifier (COA) based on the second-generation current conveyor (CCII), is proposed for redesign. This approach utilizes current-mode techniques, focusing on current rather than voltage for signal processing, resulting in lower power consumption and high-speed performance. With the IHP BiCMOS technology high-speed and linearity improvement is achievable

References

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