Low Cost Power Cycling Stimuli Generator for AMS Validation using an FPGA

– Varun Posimsetty, supervisor: Andreas Madner, Infineon Technologies, Villach

Power Cycling – Introduction

– It's the process of repeatedly turning the chip's power supply ON and OFF. Subjecting it to repeated switching for different loads stresses the chip and helps identify failure mechanism.
– Each cycle subjects the chip to an initialization phase where it must reliably reset and configure its internal circuitry for normal operation.
– Therefore it serves both a stress as well as functional test.

Motivation & Goals

– The present implementation requires multiple-waveform generators which are really expensive and only exacerbate the cost on scaling for different voltages.
– There is at least a 5 second delay in switching between different stimuli for a power cycling test of 100 millisecond.
– The goals is to build a scalable power cycling stimuli generator using an FPGA which allows users to update entries to generate different stimuli, while also addressing the issue of delay in switching between stimuli.

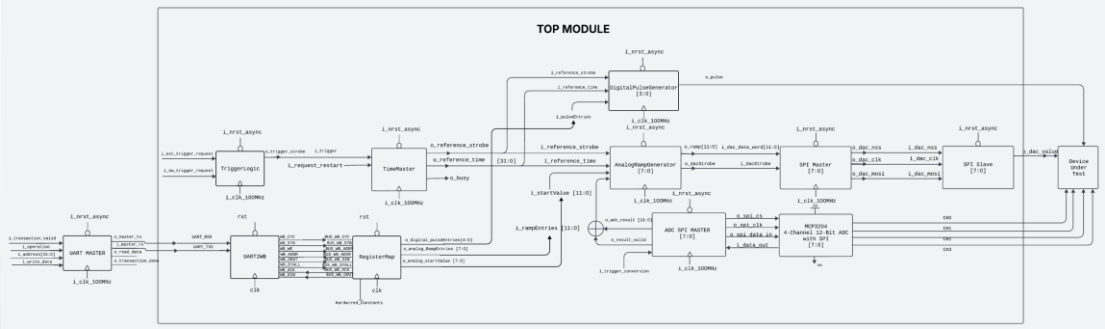

Figure 1. Block Diagram of the Top Module

Implementation & Features

– Implemented targeting an Artix-7 FPGA, generating 4 digital pulses and 8 analog ramps. The digital pulse and analog ramps are generated based of values stored in registers with the time master synchronizing the timing.
– Integrated an SPI based MCP3024 ADC for feedback to calculate errors in voltage due to IR drop at elevated temperatures.
– User can update register values using UART Master allowing for different stimuli to be generated.
– Using a single FPGA the cost is brought down from thousands of euros to just a couple of hundred, since a testbench could be fashioned in a way that register values can be altered and next set of stimuli could be entered, using the request to reset the time master can be reset and the power cycle test could continue with a delay close to 100 milliseconds.

Areas of Improvement and Future Works

– The error voltage calculated due to the IR drop and the subsequent correction is limited by clock speed of the SPI based ADC and the Baud Rate of UART.
– The current design on caters to pulse and ramp stimuli which might not be sufficient for all validation scenarios.
– Another promising direction is to implement this solution on a System-on-Chip (SoC) FPGA platform, which integrates both an FPGA fabric and a processor (ASIC) core on the same die. In this setup, the processor side can generate or update test patterns and write them to registers, while the FPGA reads and applies them in real time. The AXI (Advanced eXtensible Interface) protocol can be used to handle communication between the processor and FPGA logic, enabling more advanced control, and automation during runtime.

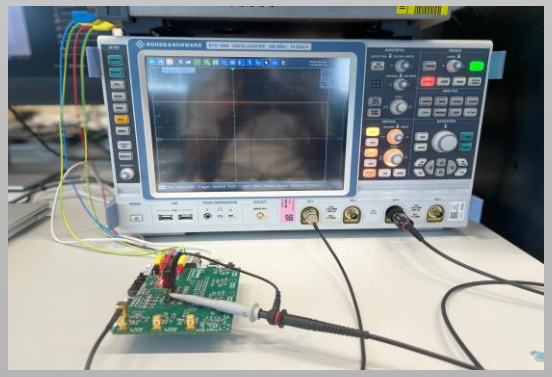

Figure 2. Test setup for waveform generation

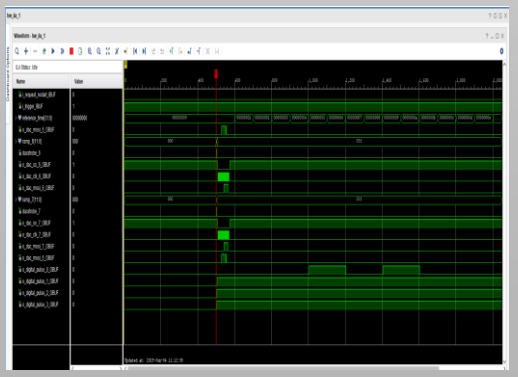

Figure 3. Xilinx Vivado HW ILA observing the pulse and ramp data transmission