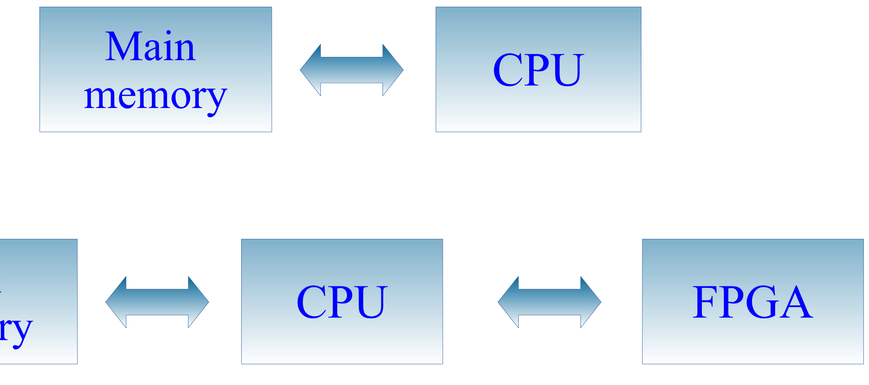
Reconfigurable processing units inside RISC-V cores

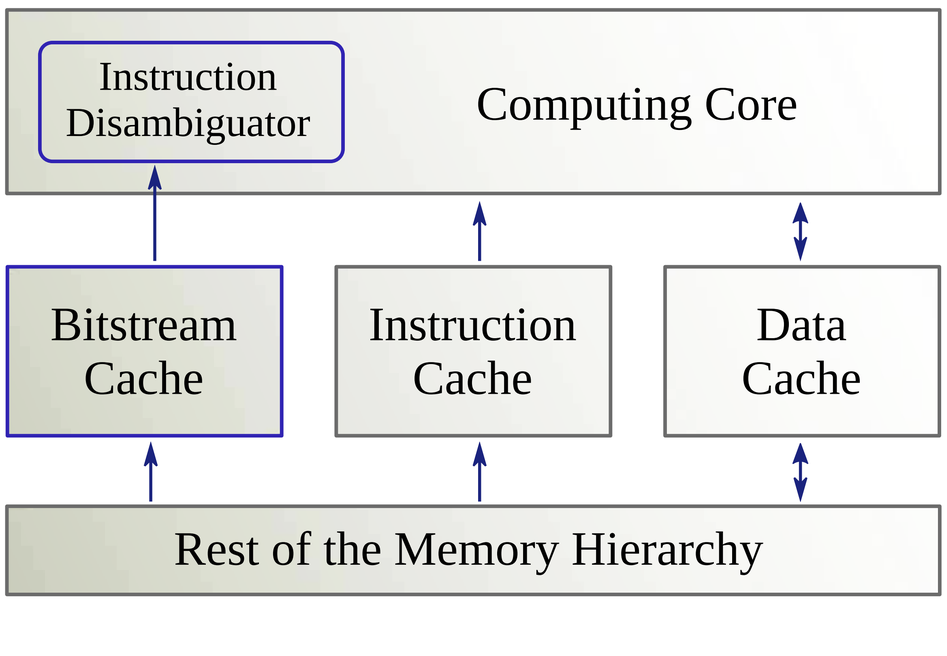
Philippos Papaphilippou

HeiChips 2025

Motivation

- CPUs are easy to program
  - Software support relatively mature
  - Programming models, libraries, portability, debug tools
  - Software and hardware abstractions, e.g. caches
- CPUs suboptimal for certain tasks. Alternatives:
  - GPUs, FPGAs, ASICs, ...
- Non-uniform memory access model (NUMA)
  - Data has to be first transferred through the CPU
  - Complications in programming models
  - Redundant and expensive hardware





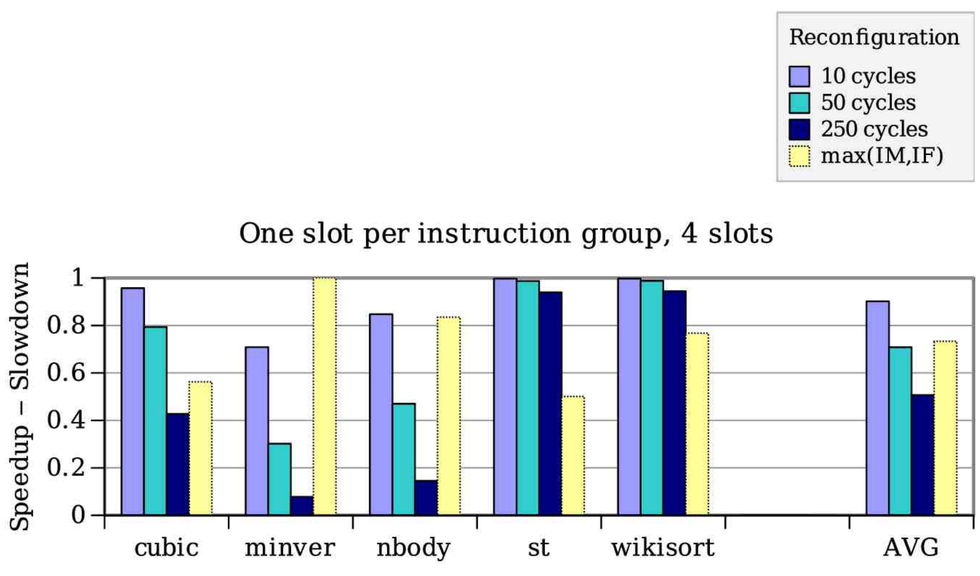
FPGA-extended General Purpose Computer Architecture [1]

- The “FPGA-extended modified Harvard Architecture”
  - A new computer architecture
  - Introduces small FPGAs in modern CPUs
- Comprehensive evaluation of instruction-level reconfiguration
  - For single and multi-processing with an operating system
  - Based on Simodense [2] (in-house RISC-V softcore)
- Feasibility studies

COMPARISON OF OF THE PROPOSAL TO EXISTING COMPUTER ARCHITECTURES

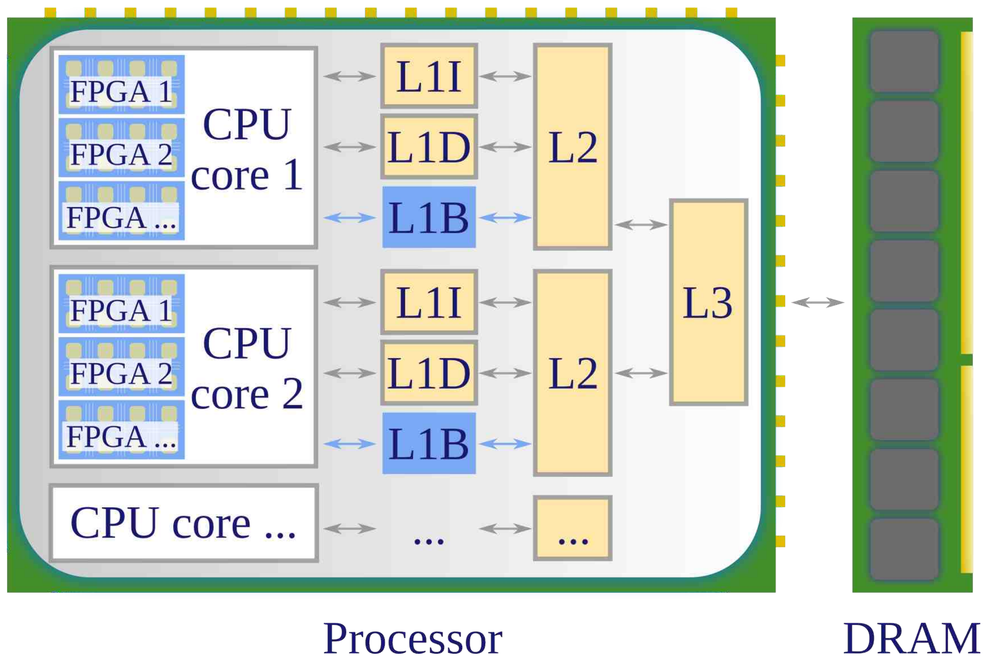
Computer Architecture	Von Neumann	Harvard	Modified Harvard	Conventional Heterogeneous (Modified Harvard)	FPGA-extended Modified Harvard
L1 datapaths	Shared between I/D	Separate for I, D	Separate for I, D	Separate for I, D, (B)	Separate for I, D, B
Address space/ L2+ datapaths	Shared between I/D	Separate for I, D	Shared between I/D	Shared between I/D, Separate for B	Shared between I/D/B
Memory performance	Low	High	High	High for I/D, Low for B	High

Legend – I: instructions, D: data, B: bitstreams



Ongoing research

- Fine-tuning of the CPU core architecture
- Fine-tuning of the internal FPGA architecture
- Optimising bitstream format
- Instruction-level parallelism
- Out-of-context execution
- Software support
- Operating system support
- Tape-out of a demo chip



University of Southampton

Source code: philippos.info

[1] Philippos Papaphilippou, Myrtle Shah "FPGA-extended General Purpose Computer Architecture" The 18th International Symposium on Applied Reconfigurable Computing (ARC) 2022

[2] Philippos Papaphilippou, Paul H. J. Kelly and Wayne Luk "Simodense: a RISC-V softcore optimised for exploring custom SIMD instructions" FPL’ 2021