Ever wanted to design your own ASIC in VHDL?

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This project investigates the implementation of a digital storage oscilloscope (DSO) on an application-specific integrated circuit (ASIC) using Tiny Tapeout. By employing modular design and open-source tools, it addresses challenges such as limited on-chip memory and the specific constraints of ASIC design. The outcome demonstrates the feasibility of compact and functional ASIC development, integrating features like video output, external F-RAM buffering, and a test signal generator.

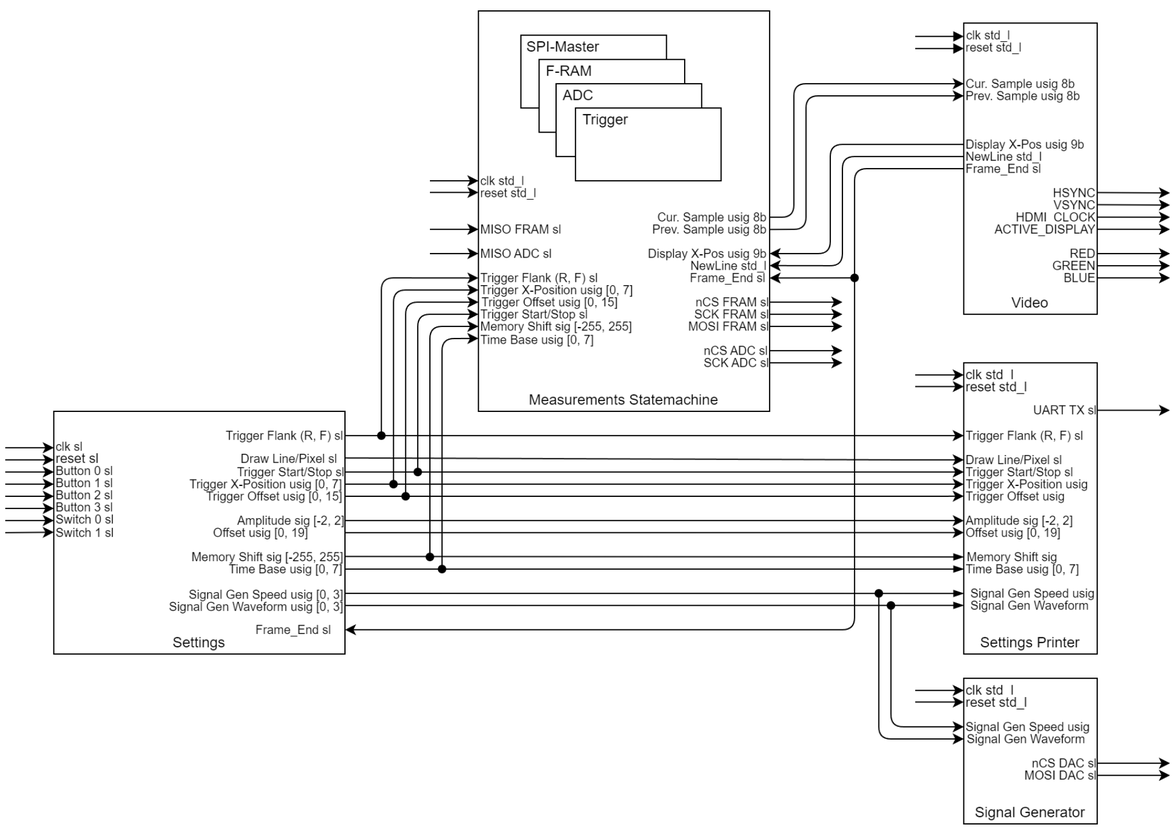
Materials & Methods

The project utilized hardware components such as FPGA boards, Pmod modules, and F-RAM chips alongside software tools like Tiny Tapeout, Visual Studio Code, NVC and GHDL to design, simulate, and test the digital storage oscilloscope's functionality and performance. All Pmod modules from the VHDL DSO semester project had to be used.

Challenges

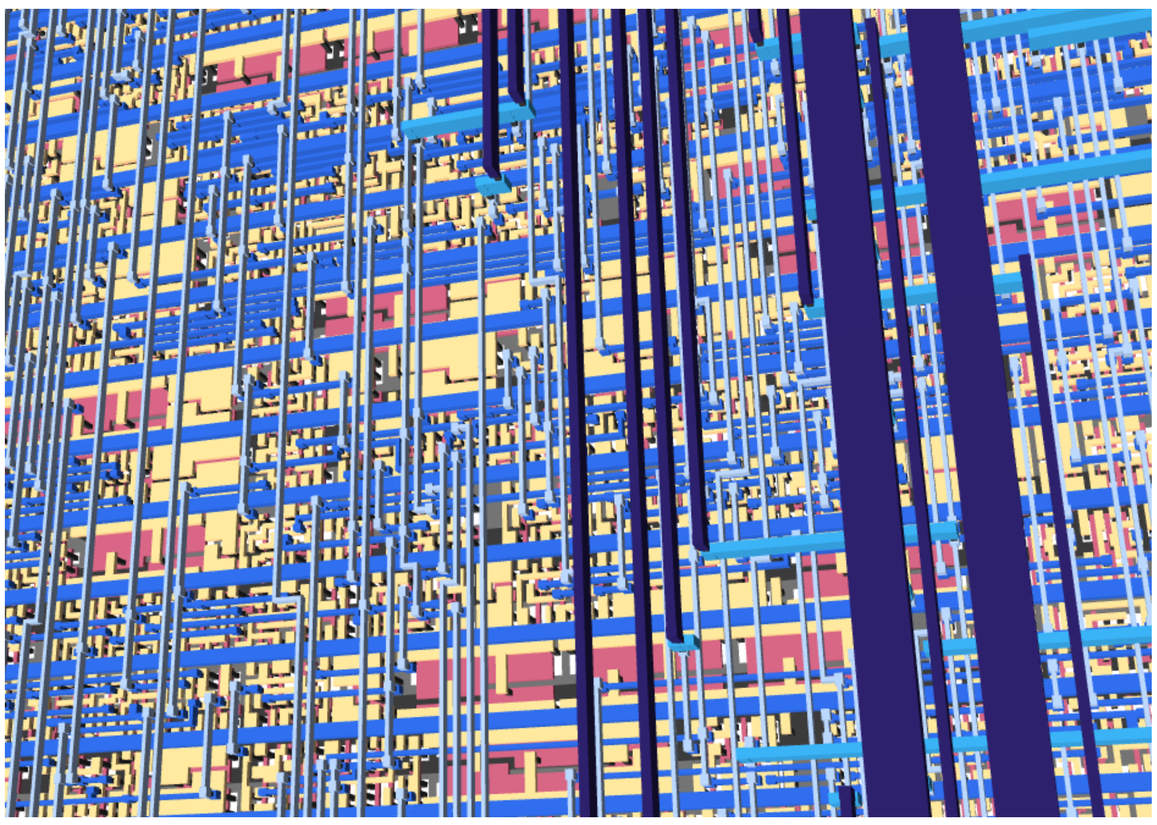
Designing an ASIC using the Tiny Tapeout tools posed several challenges. The limited memory and storage of the ASIC required significant design adjustments compared to FPGA implementations, requiring optimization to fit within the constrained tile area. The restricted number of I/Os demanded careful allocation and adaptation of the interface design to balance functionality and robustness. Additionally, the six-week timeframe imposed strict deadlines for planning, implementation, and verification, adding to the complexity of the development process.

Design



The design incorporates a modular and robust system featuring ADC inputs, a video generator for display output, external F-RAM for signal buffering, and UART for configuration monitoring. It achieves VGA-compatible output with a rotated display to minimize memory usage and includes a versatile test signal generator alongside real-time setting adjustments.

Result



ASIC Resource Utilization:

• ASIC Utilization	68.57%
• Total Flipflops	232
• Logic Gates	2316
• Transistors	24’597

The tests on the FPGA performed without issues and the ASIC synthesis report demonstrates a successful translation of an VHDL-based design to an ASIC.

Conclusion and Outlook

This project was an exciting opportunity to design an ASIC as a student. Tiny Tapeout made the process easy by simplifying installations through GitHub Actions, allowing for syntax checks with TerosHDL and NVC, and synthesis on GitHub with every push. Despite the limited resources on the ASIC, such as memory and registers, and the tight 6-week timeline, the project was completed successfully, making this an enriching experience.

The ASIC will arrive after the completion of this project, at which point evaluating the received ASIC and comparing its performance to the FPGA simulation will take place. Future work based on this project could involve optimizing the SPI communication for enhanced I/O availability, integrating additional analog input channels or exploring advanced user interfaces for easier configuration.

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