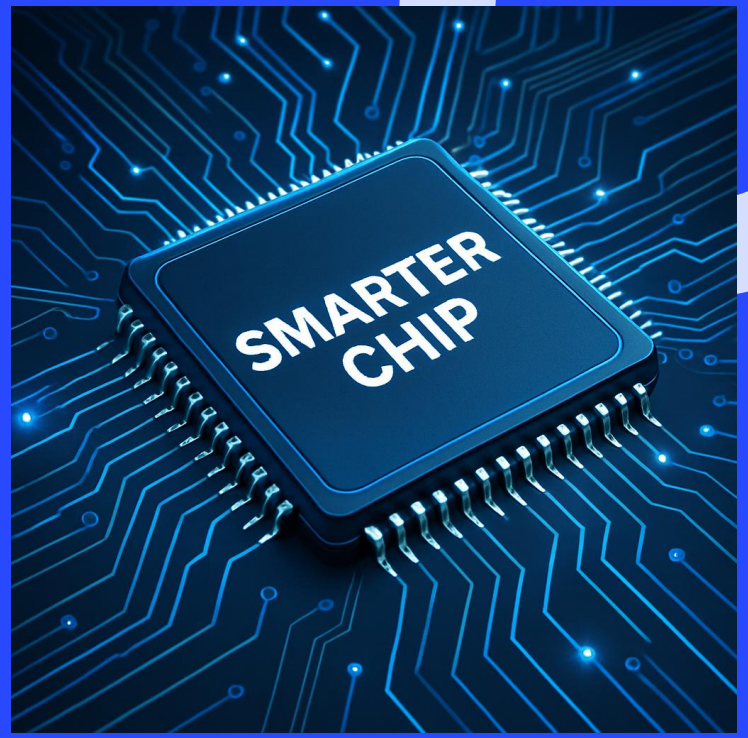
Smarter Chips, Healthier Lives

Dr. Veena S Chakravarthi

Agenda

- Smarter Chips
- AI adoption in chip design
- Open cores and Open-Source tools
- Healthier Lives

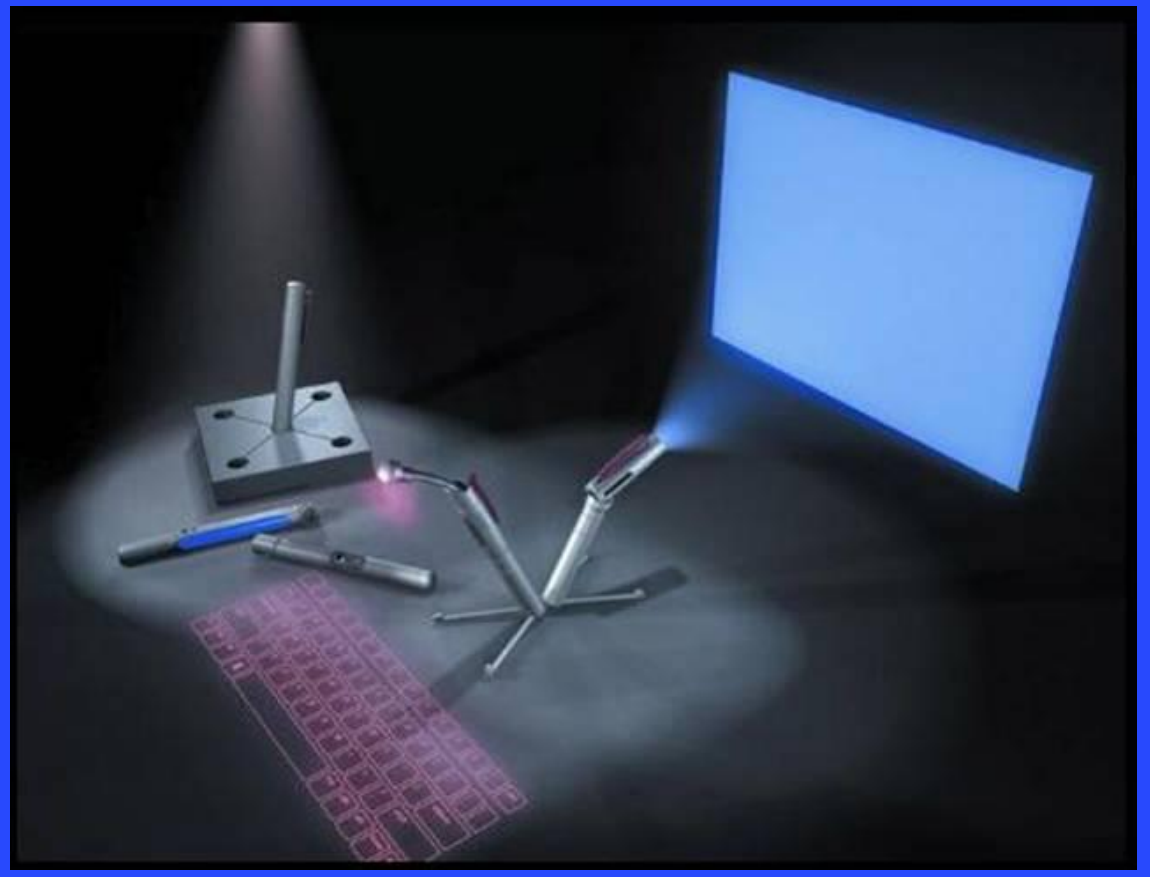
Smarter Chips ‘SOC to Solution’



Guess what ..

Look closely n' guess what they could be.....

Product

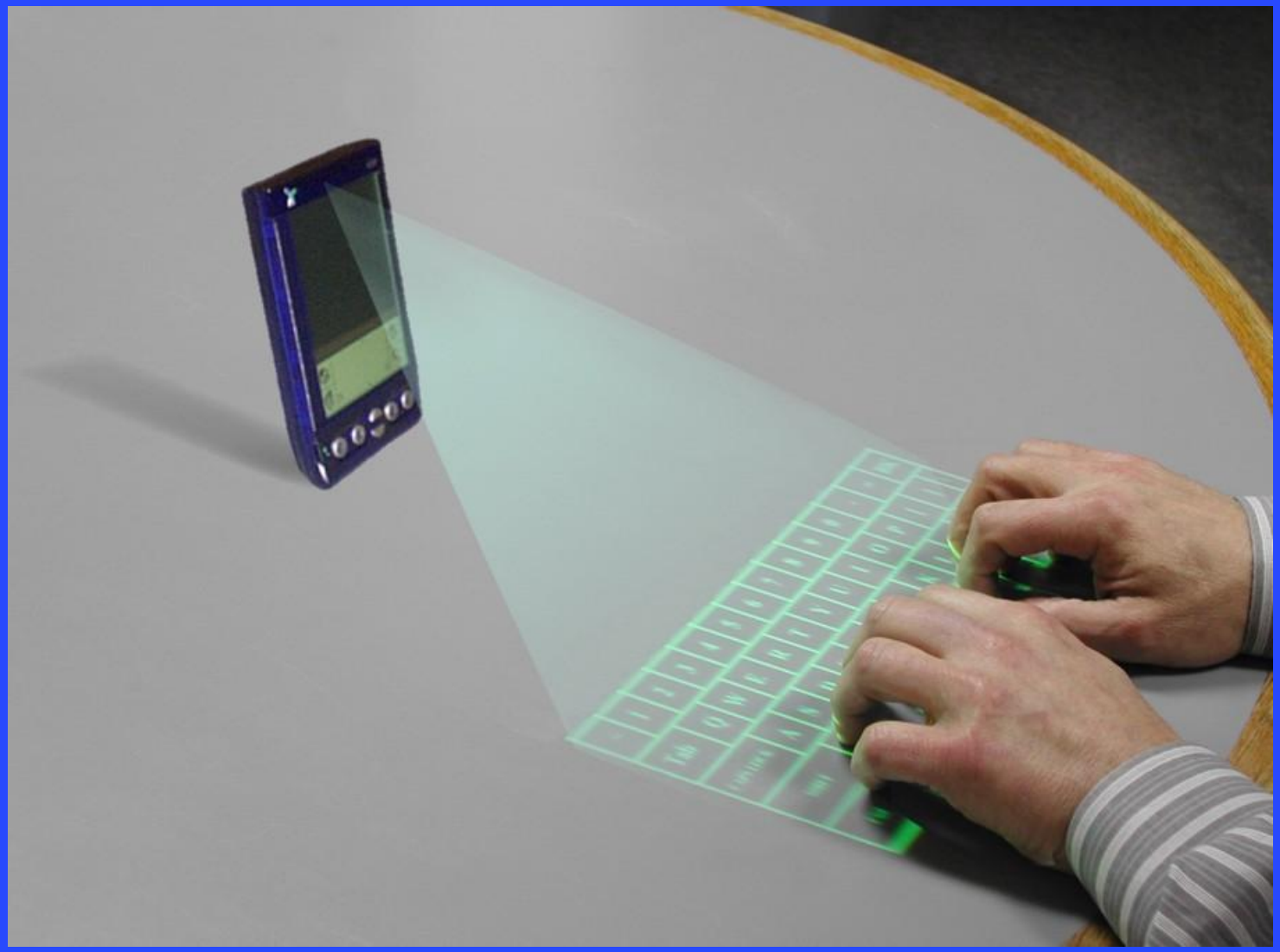


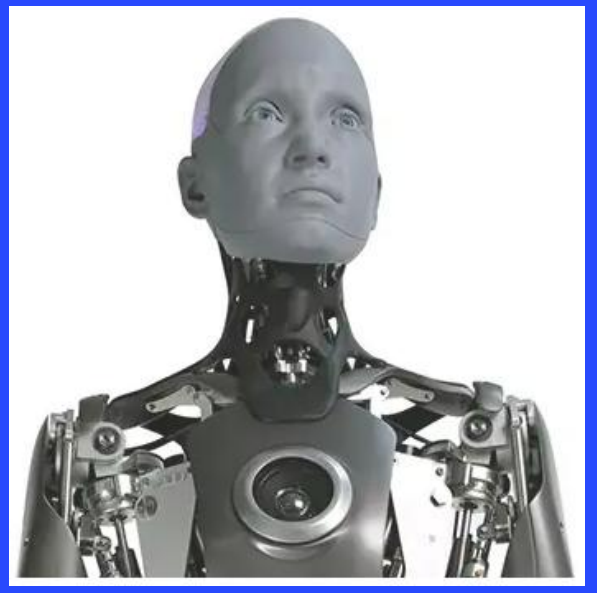
Guess what..

Product

Guess what..

Product






SKYDRIVE


Freedom

Apple will continue to replace suppliers' technologies with their own.

Companies such as Google, Meta, Amazon, and Microsoft, reduced dependency on third-party silicon (NVIDIA, AMD, Qualcomm) to optimize for their workloads.

Harnessing **DeepMind's reinforcement learning** to optimize chip design and data center efficiency

The **overall AI chips market** is expected to reach **nearly USD 93 billion in 2025**, and exceed **USD 100 billion by early 2026**.

News around us

Largest AI disruption will shift chip design in this legacy industry, and Cognichip is leading it with a level of intelligence and precision we've never seen before in chip design

Fully transitioning its smartphone SoCs (Tensor) to **in-house design and TSMC fabs**

Smart Everything: Industries Will Be More 'Intelligent' Than Ever .

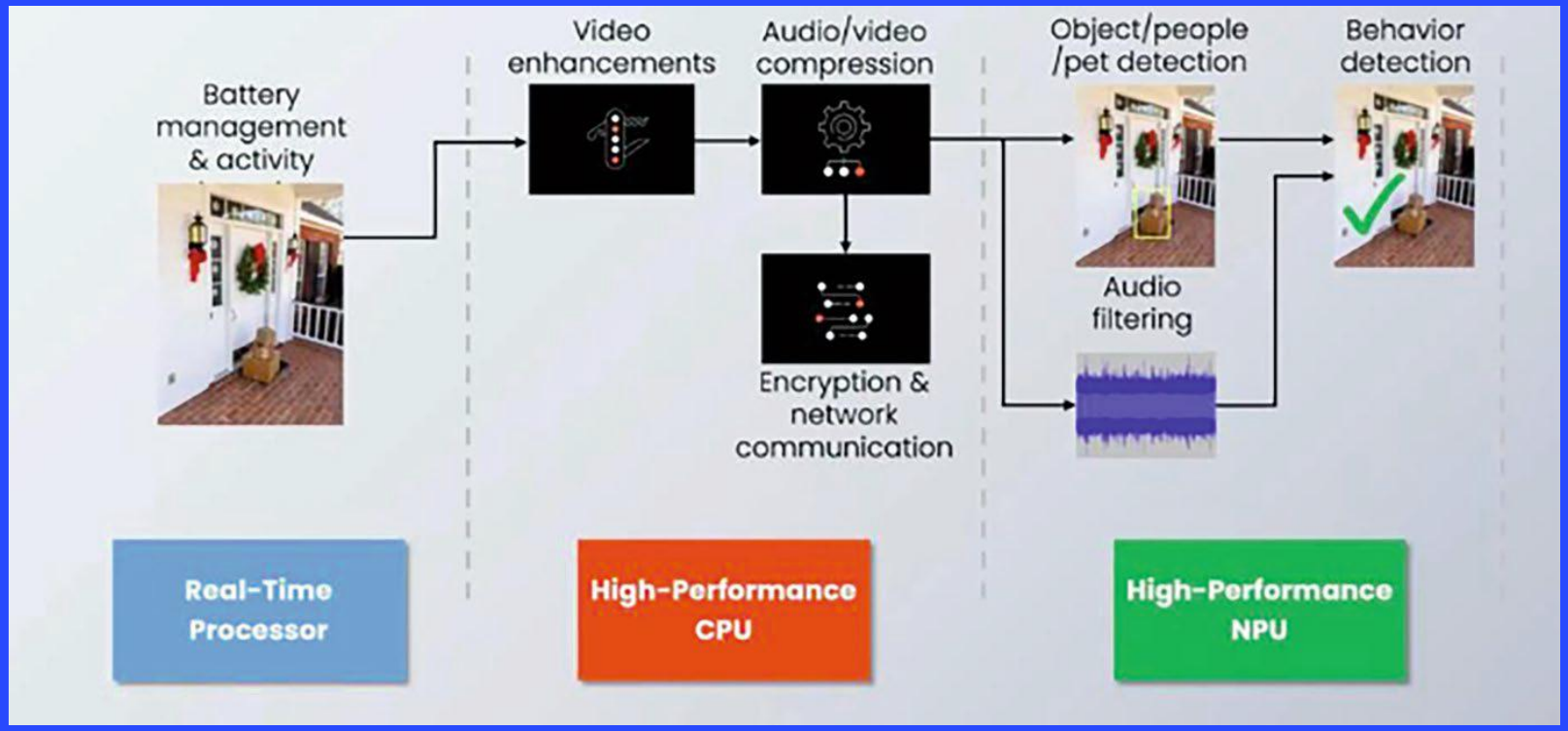
TSMC has officially confirmed plans to open its **first chip design center in Europe**, located in **Munich, Germany**, scheduled to begin operations in **Q3 2025**. The new facility will support European customers with **high-performance, energy-efficient chip design**, focusing particularly on applications in **automotive, industrial, AI, and IoT** sectors

The CHIPS and Science Act: While billions in funding are being disbursed to boost semiconductor manufacturing and research, there's debate about expanding the scope of tax credits to include upstream material suppliers.

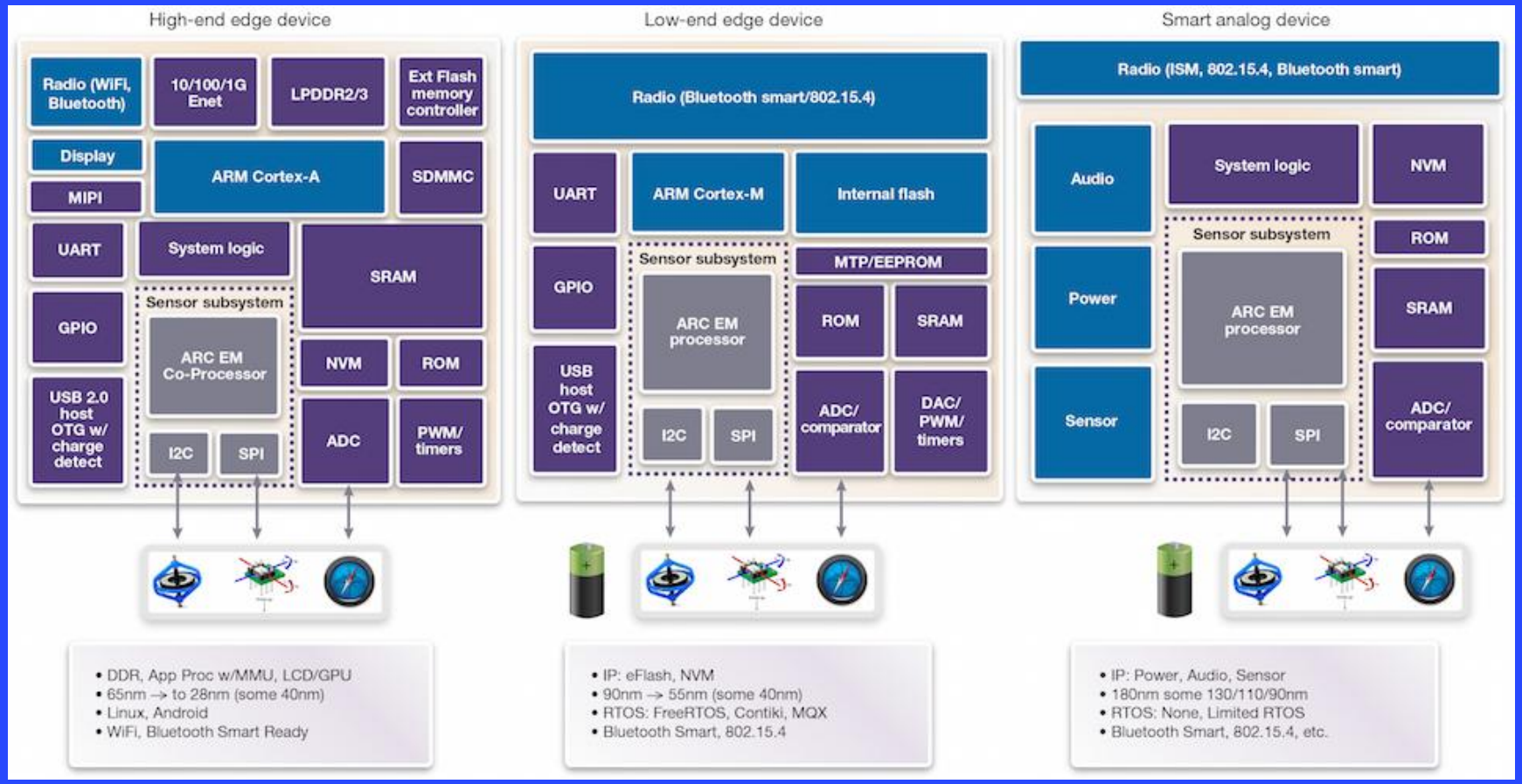
AI SOC design

- Custom chips are being designed with AI acceleration at the core
- Dedicated AI engines and specialized cores to handle neural network computations efficiently
- Domain-specific architectures are becoming standard.
  - Google’s TPUs are optimized for machine learning at scale.
  - Meta’s MTIA chips deliver efficient inference for large language models in social and metaverse platforms.
  - Microsoft’s Maia chips target training and inference in Azure.
- Optimized performance for training and inference tasks across a range of AI applications, from large language models to edge AI devices.
- Chip design is now about innovation at every level, from architecture and packaging to energy efficiency and security.

AI Solution throughout



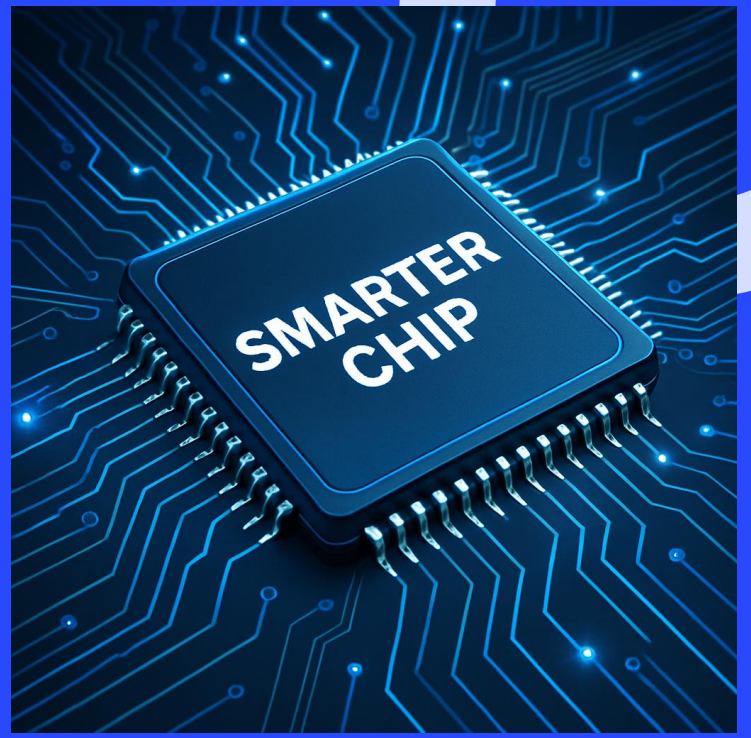
SOC Architecture



Takeaways

- Everything is smart and intelligent
- Systems are small to large
- System requirements are domain specific
- Complexity increased manyfold
- Reusable ratio phenomenal
- Knowledge of everything
- Change in design methodology
- Complete Solution in product form
- …

Open Cores
Open-Source Tools



Problems addressed

- Cost of proprietary EDA tools
- License restrictions
- Limited access to cutting-edge IP for startups and academia

Why open-source matters:

- Transparency, flexibility, cost
- Enabling custom core development
- Synergy with Linux-style development ecosystems
- Hands on resources for everyone to design chips at no/low cost

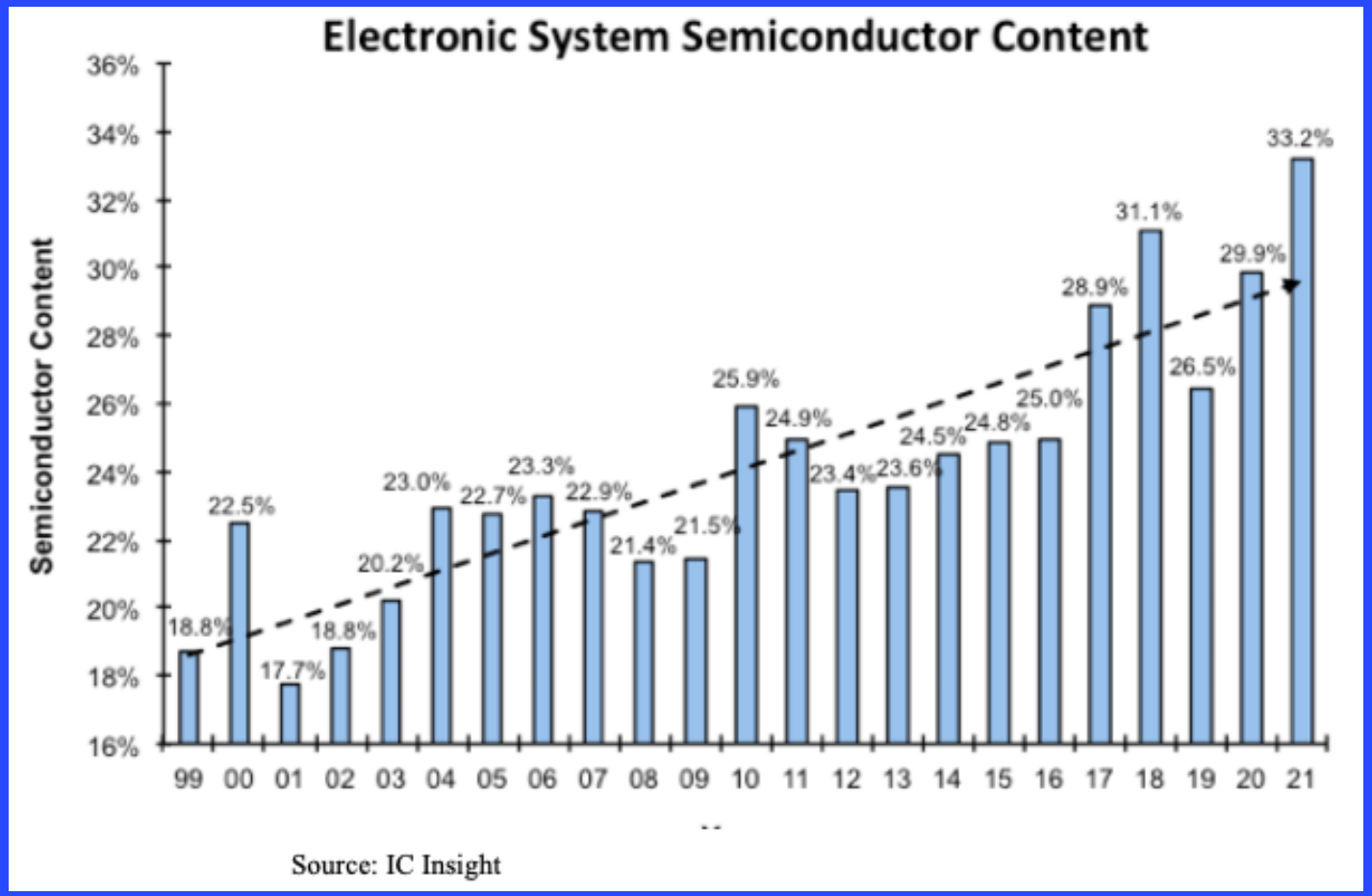
Open Core vs Linux Eco system

Open-Source Kernel (Linux)	**Open ISA (RISC-V)**
Modular Architecture (Kernel + Drivers) Each part can be built, tested, and improved independently	**Composable SoC Design (Core + IP blocks + Interconnect)** SoC blocks (cache, bus, memory, peripherals) are modular and replaceable
Version Control: Git, Patches, Branching Collaborative development via Git workflows	**Git-managed RTL Repos: RocketChip, CVA6, etc.** RISC-V cores and SoCs follow same workflows with PRs, forks
Distribution: Debian, Fedora, Arch, etc. Linux distros with different goals and configs	**SoC Variants: Ariane, SweRV, PicoRV, Shakti, etc.** RISC-V SoCs tailored for performance, size, or power
Toolchains: GCC, LLVM, Buildroot Open compilers and build systems	**EDA Toolchains: Yosys, OpenROAD, Verilator, GHDL** Open synthesis, simulation, layout, and verification flows
Packaging: Docker, CI/CD Pipelines Simplified reproducibility and testing	**EDA-in-Container: Docker + GitHub Actions for RTL Flows** SoC flows containerized for quick setup and scalability
Community Contributions & Maintainers Patches from individuals, universities, companies	**Hardware Maintainers & GitHub Contributors** IP contributions and fixes from global contributors
Governance: Linux Foundation, Maintainers Structured but inclusive governance model	**RISC-V International, Chips Alliance, FOSSi** RISC-V ecosystem mirrors similar foundation-based governance
Ecosystem Tools: GDB, Valgrind, Strace Tools for debugging and instrumentation	**SoC Debug Tools: Spike, QEMU, GDB for RISC-V, Tracers** Open simulators and debuggers help analyze SoC execution
Documentation and Forums Encourages self-learning and transparency	**Markdown Docs, Wiki, Forums, Mailing Lists** Encourages learning and independent SoC design from scratch

Open Core Democratization stack

- **ISA**: RISC-V
- **HDL/RTL**: Chisel, Verilog, SystemVerilog, VHDL
- **EDA Tools**: Yosys, OpenROAD, Verilator,
- **Simulation**: Verilator, GHDL, Gtkwave
- **Emulation**: Spike, QEMU, Renode, OpenOCD
- **Software Stack**: GCC/LLVM, Clang, Zephyr, Linux, FreeRTOS
- Bootloaders: OpenSBI, U-Boot and Bare metal bootloaders

Semiconductor content in systems



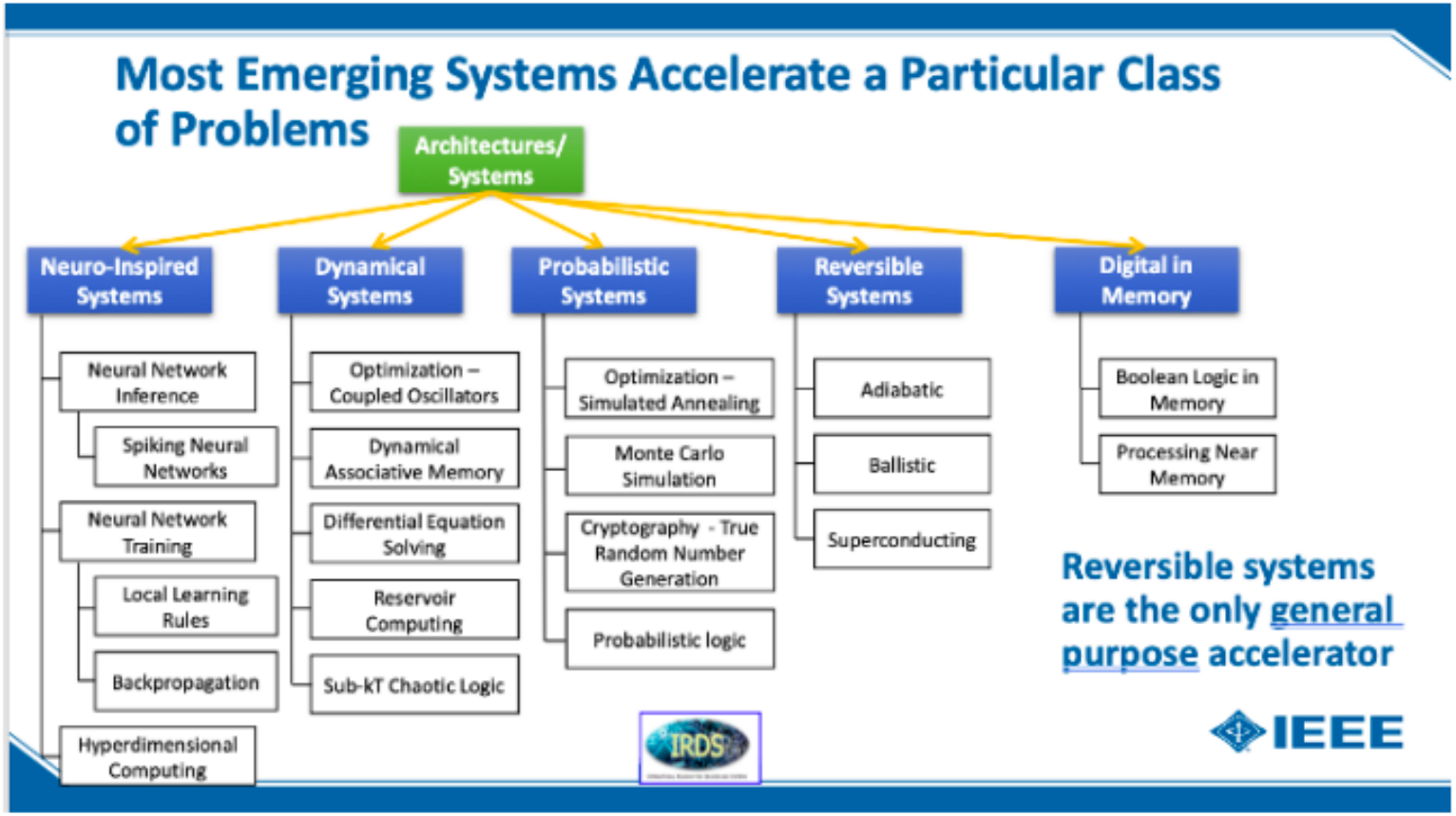


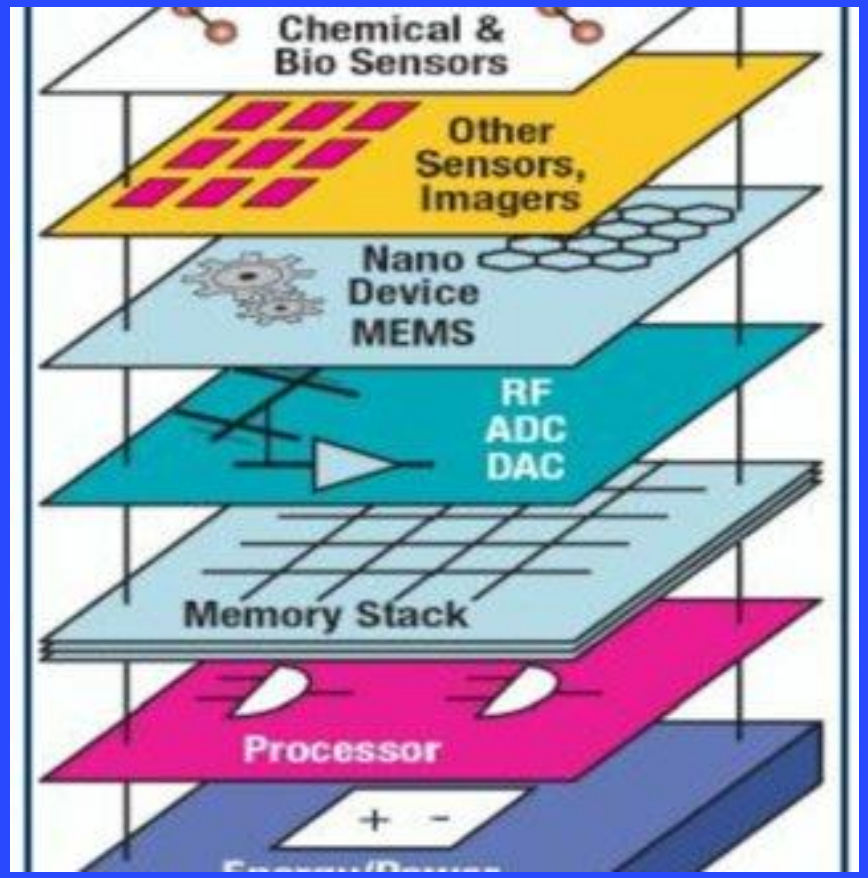
Figure ES33 *Multiple specialized architectures are emerging to solve specific problems*

Future Systems

- Impossible to find single component providing all functions
- Increased system complexity as number of sub systems increase
- System integration is a dynamic process continually evolving
- It may be economical to build large systems out of smaller functions separately packaged and interconnected
- Monolithic homogeneous or heterogeneous integration at the die level or heterogeneous integration at the package level are tools selected as appropriate on a case-by-case to optimize system performance and minimize cost

Future Systems

- Outside system connectivity important.
- The key challenges for radio frequency (RF) are to achieve high-performance
- Need energy-efficient RF analog technology compatible with CMOS processing and delivering capabilities to support a broad range of applications for IoT devices



Solution approach

- Identify problem of interest
- Explore probable solutions
  - Analyze existing solutions
  - Improvisation vs Radically novel
- Model solution
  - Identify modeling framework
  - Tool platform
  - Available subsystem models
- Identify hardware system/s
  - Identify subsystems
  - Types of subsystems
  - Technology of the subsystem components
  - Integration plan
  - Verification at subsystem/system level

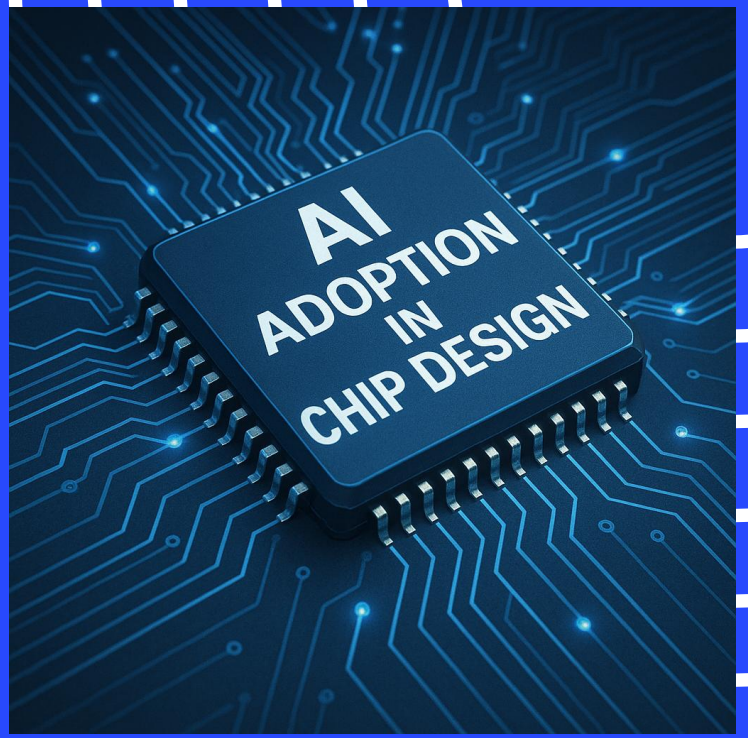
Solution approach

- Design and development plan
  - Hardware development
  - Software development
- Prototyping for POC
  - Validation against intended requirements
  - Feedback changes in specification
  - Define development plan
- Tips:
  - Explore open cores at all levels
  - Explore verification platforms

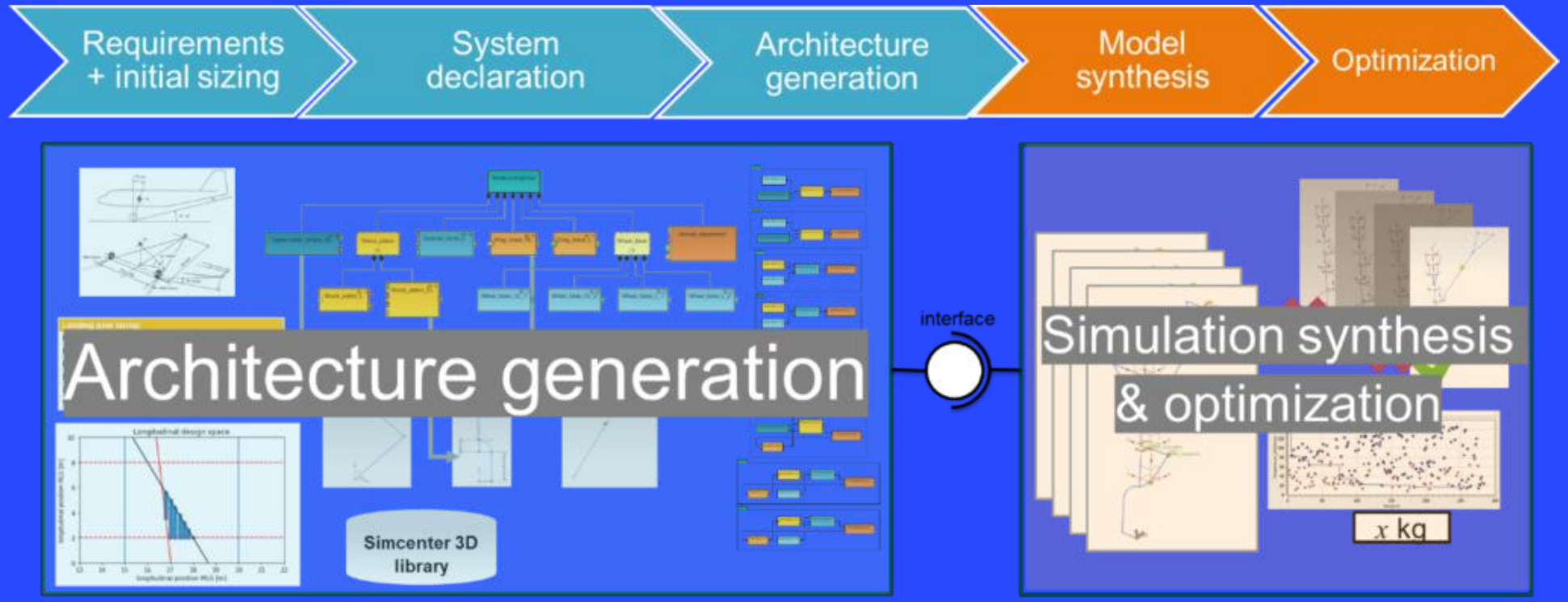
Chiplet - Based Design & Heterogeneous Integration

- **Chiplet Architecture**: Breaking large monolithic dies into smaller chiplets for yield and flexibility.
- **Standards**: Explore UCIe (Universal Chiplet Interconnect Express) for interoperability.
- **Advantages:** Cost reduction, modularity, mixing nodes (e.g., analog on mature nodes, logic on advanced nodes).
- **Use Cases**: High-performance CPUs, GPUs, AI accelerators.

AI adoption in Chip design



EDA technology trends



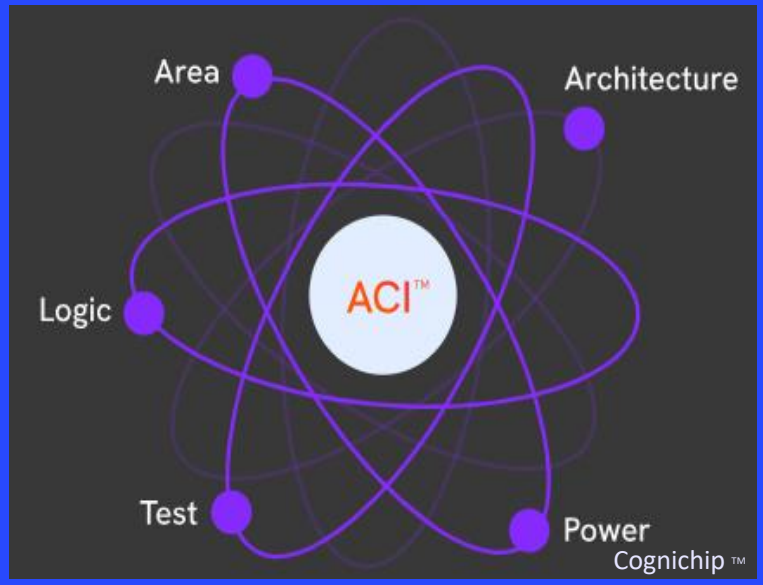
Source: Siemen's blog

EDA technology trends

- Cloud as a computer
- Increase design reuse ratio with library of open cores
- AI based Design space exploration
- Smarter EDA, simulation and system level modeling tools
- Design for context requires EDA tools with greater interoperability, computer-aided design (CAD), computer-aided engineering (CAE), and test tools.
- Design and development framework better integration of EDA tools with product lifecycle management (PLM) systems

AI adoption in SOC design

- AI is getting adopted to design the very chips that power AI systems.
- Machine learning models are employed to generate designs, optimize floorplanning, timing closure, and layout, dramatically reducing design cycles from weeks to hours.
- Reinforcement learning techniques are effective in automating complex chip design steps, improving overall power, performance, and area efficiency.
- AI-driven electronic design automation is a critical enabler of next-generation SOC development.
- AI has introduced two other optimization factors in chip designs; Cost and TTM



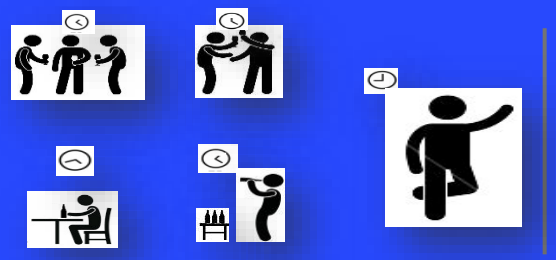
Follow https://www.cognichip.ai/

Healthier Lives

The Problem

No real time feedback. No Historical data

No Easy Access to Data/Analysis. Just to manage vitals, need to visit doctor



Challenge to manage social life with chronic disease

Multiple devices and systems

Our Solution

- SenseSemi Products & Ecosystem

Gen-1

Gen-2

SENSESMART
SENSEHEALTH
SENSELAB

* Blood Glucose
* Blood Pressure (Cuffless)
* SpO2
* ECG (Up to 6-Lead)
* Wireless ECG Patch

* Body Temp
* Alcohol Sensor
* Digital stethoscope
* Sweat Sensing
* Lab on Chip

SENSESMART APP
Android/IoS

SENSESEMI HEALTH ANALYTICS

DOCTORS/HOSPITALS NETWORK

SENSESEMI WEB INTERFACE FOR DOCS/HOSPITALS

Business Model

Chronic Disease management

-Monitoring the Vitals
-Recon based on Analytics

-Remote Vital Monitoring
-Patient Data management
-Analytics & AI

-Remote Monitoring
-Post Operative care

-Drug Trials

Doctors

Hospitals

Pharma/ Insurance

-Patient Data management
-Analytics & AI

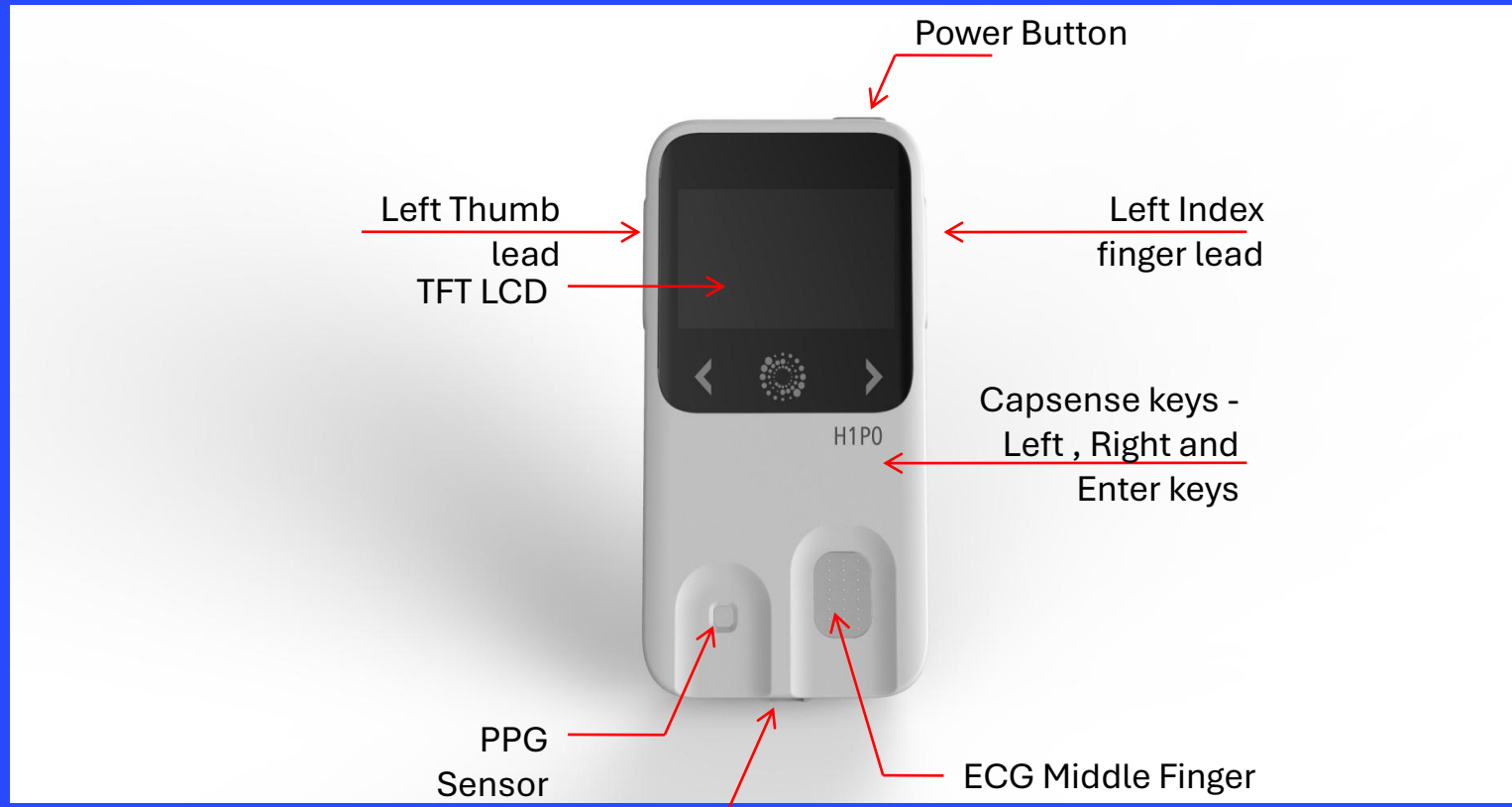
- Data/Vital Acquisition
- Analytics & AI
- Subscription

-Bulk Subscription
-Patient Data management
-Analytics

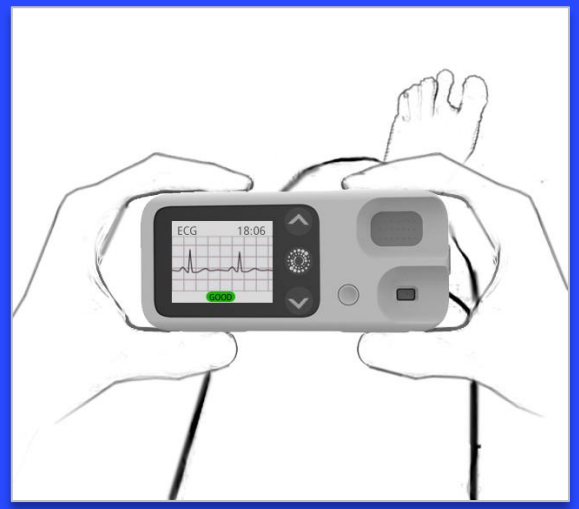
- Subscription
- Patient Data management
- Analytics & AI

SENSE SEMI

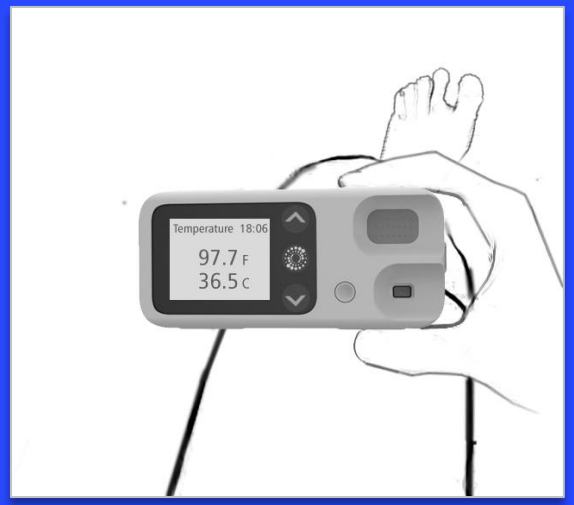
SenseProtoH1p0



How it works?



ECG



Temperature

BP

Blood Glucose

Affiliation Awards and Recognition

Awarded One of the Top Tech 25 Companies for the year 2016 by Govt. of Karnataka & KBITS

- SenseSemi was Shortlisted among top 20 IoT Companies from IESA in IoT Next Conference
- SenseSemi has 6 Patents in US & India in these technologies
- Clinical trials on POC conducted in two Hospitals with Positive feedback

My Learnings…

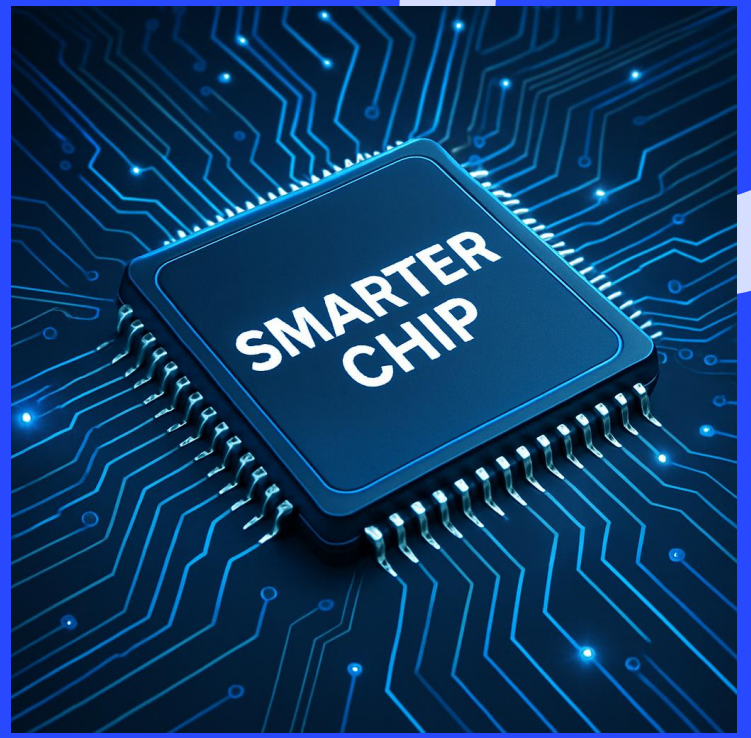
1. Lead with “why”. Start with a purpose, not because you have mastered technology.
   - Sensesemi was founded to solve chronic health management
2. Be T-shaped
   - Deep expertise in one area e.g. chip design(open cores), broad in others such as AI, healthcare, automotive, cloud. Multidiscliplinary innovation has many advantages today than siloed expertise
3. ‘Invert—always invert.’ “Invert” means: Instead of asking, “How do I succeed?” , ask “What would cause me to fail?”
   - Instead of “What makes a good SoC?” — ask “What makes a bad one, and how do I avoid it?” It’s a way of eliminating errors, blind spots, and overconfidence
4. Embrace Open Source & AI Tools
   - Democratize Innovation. Use, learn, contribute
5. Convert Information into Wisdom
   - It is Retrospection with Application. This enables you to think what you don’t know.
6. Be a Mentor and Mentee
   - Always seek guidance, Share your learnings with peers, juniors. Create value in the community.
7. Build, Don’t Just Learn
   - Our Real-world projects teach resilience. MVP of a health device > theory alone. Iterate, test, fail fast.

Learnings…

8. Ethics Over Everything
   - This is true everywhere and especially critical in healthtech. Security is the absolute requirement. It is said that long-term non-stupidity is the long-term advantage. Show your integrity over knowledge.
9. Build, Don’t Just Learn
   - Our Real-world projects teach resilience. MVP of a health device > theory alone. Iterate, test, fail fast. Commit to Continuous Learning
   - Prototype Early, Dream Big
   - Don’t wait for funding. Today you have access to so many opensource tools and resources such as cloud credits, sandboxes. Build your idea’s first version and iterate using them.
   - Most important mantra is ‘Learn, unlearn, relearn.’ Pick one new tech every 2 years. I have worked on Communications, EPON, WLAN, Bluetooth, New-gen WLAN, MEMs, Body vital monitoring technologies in healthcare , EDA tools and now AI SoCs as domains
10. Build Your Network Engine
    - Your network at ‘Heichips summer school, your professors, industry experts, young researchers, online community peers’ is your intellectual capital. Nurture it.

What LeadSOC does?

www.leadsoc.com



Overview of Contents

LeadSoC Overview

Engineering Strength

Leadership Team

Service Offerings

VLSI Frontend Design

Embedded & Platform SW design

Full-Stack Application Development

VLSI Backend Design

DSP SW Design

Scalable Backend Design & Devops

System & PCB Design

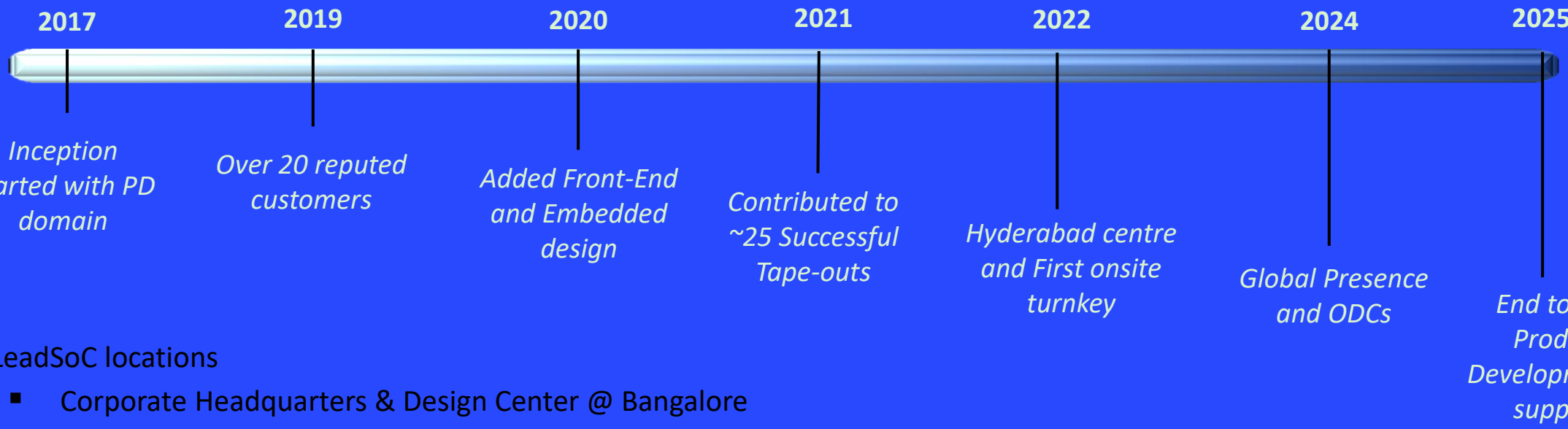
Automotive SW Competency

IOT, Big Data Analytics and AI/ML Applications

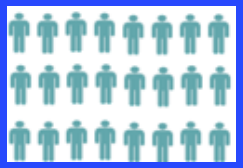
Engagement Models

LEADSOC Company Overview

Our Journey



630+
Resources



- LeadSoC locations
  - Corporate Headquarters & Design Center @ Bangalore
  - Engineering Centers : Hyderabad – 100+ engineers and Noida – 15+ engineers
  - Sales Center @ Berlin & California
- Comprehensive VLSI Solutions and Services
- Involved in multiple complex SoC Projects (Physical Design, SOC Sign-off, RTL Design, Verification, Emulation & Validation) in technologies from 65nm to 2nm
- Extensive experience in Embedded, Application SW and end-to-end HW (System Design & PCB)
- Committed to Quality, Transparency, and Continuous Improvement

LEADSOC Advantage

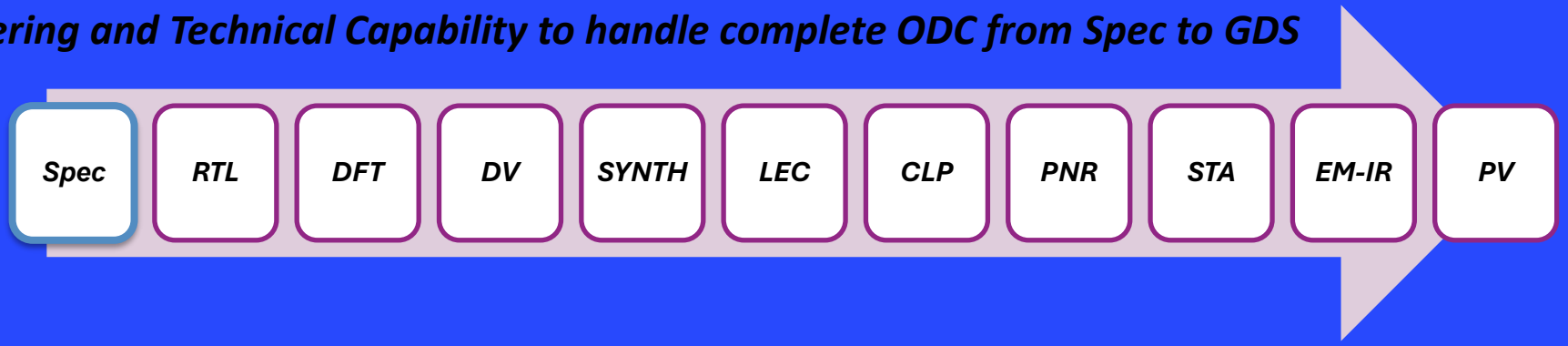
Trust: *7 years of partnership and transparent relationship with Customers*

Management Commitment: *Leadership is fully engaged to make partnerships successful*

Agility: *Compared to larger service competitors, our response will be nimble*

Expertise: VLSI *(PPA techniques like Fully Abutted Tile Flows, Advanced CTS techniques, Low Power Implementation & Checks, RISC V)* ***and Embedded*** *(RISC V, Secure Boot, RTOS, Protocol Stack, etc)*

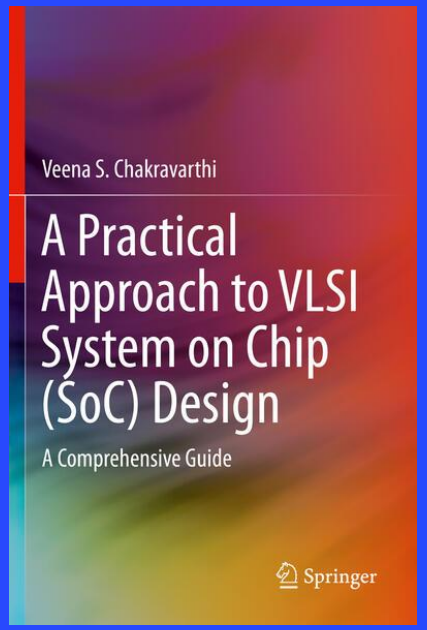
Engineering and Technical Capability to handle complete ODC from Spec to GDS

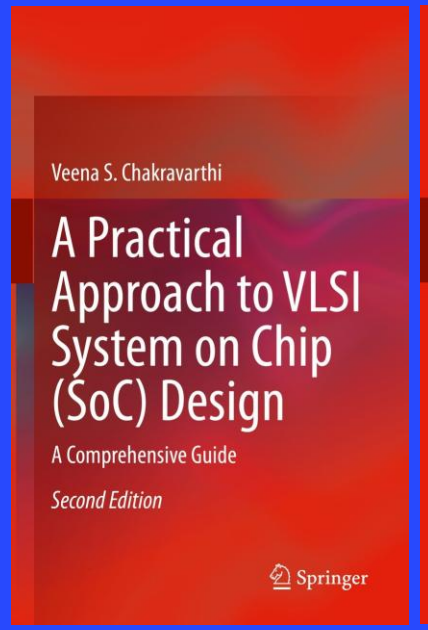


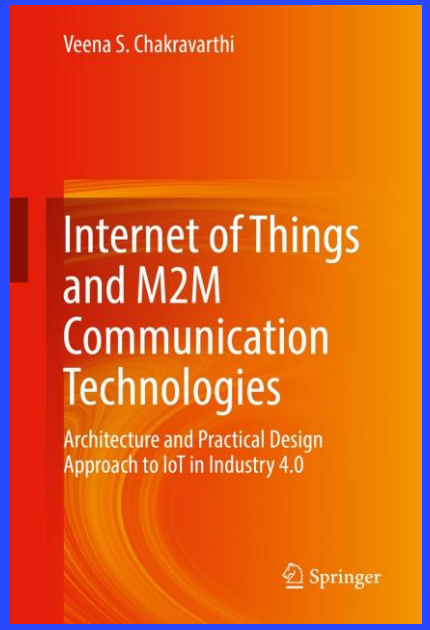
Engineering and Technical Capability to handle Embedded Software across domains

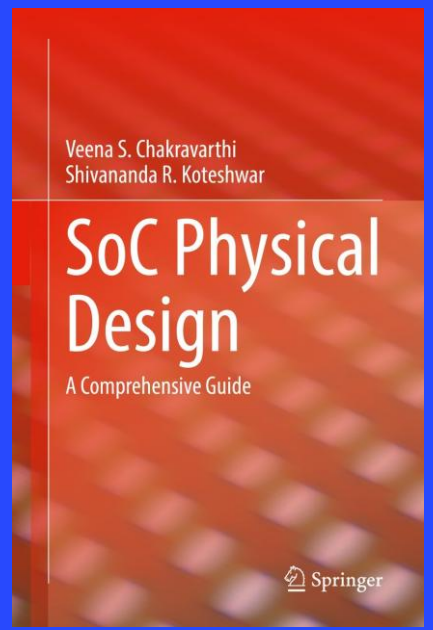
You may refer to…

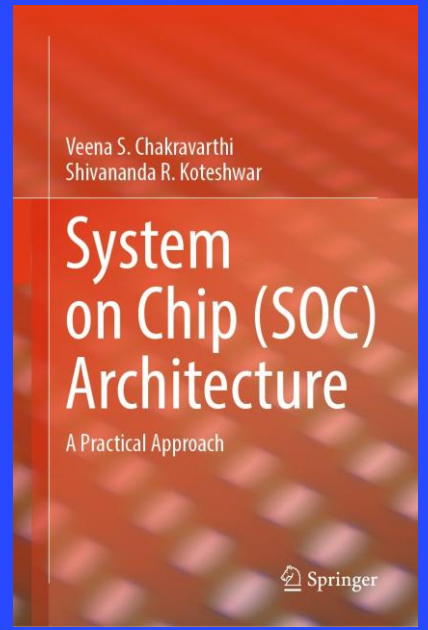
- https://link.springer.com/book/10.1007/978-3-031-18363-8
- https://link.springer.com/book/10.1007/978-3-030-98112-9
- https://link.springer.com/book/10.1007/978-3-030-79272-5
- https://link.springer.com/book/10.1007/978-3-031-85044-8
- https://link.springer.com/book/10.1007/978-3-031-36242-2

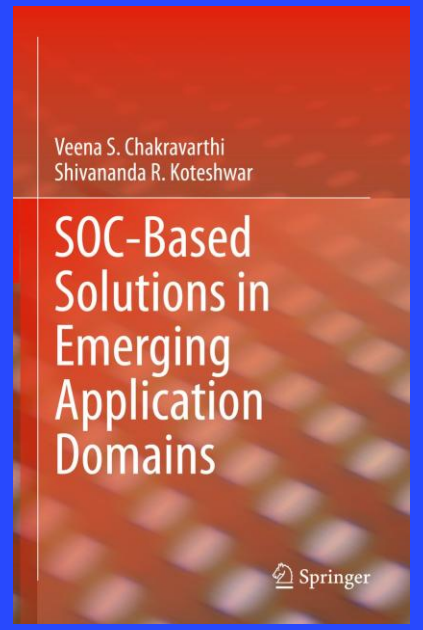












Thank you

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