FPAAs & 130nm Std Cells & Tools

Georgia Institute of Technology (ATL & Metz)

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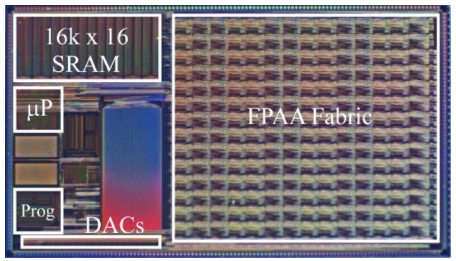
School of Electrical and Computer Engineering

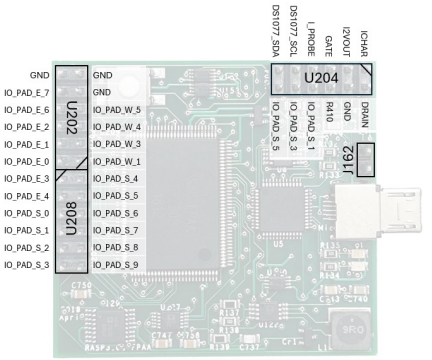
TUESDAY SESSION: FPAAS & 130NM OPEN-SOURCE CELLS

SoC FPAA devices

https://hasler.ece.gatech.edu

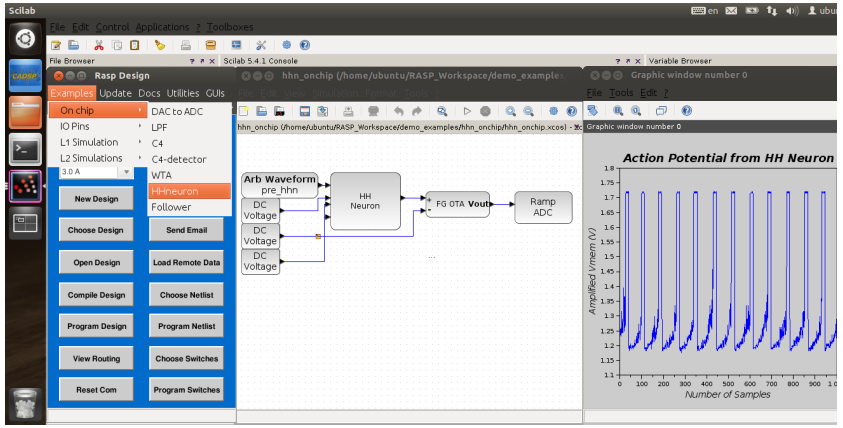
https://hasler.ece.gatech.edu/Courses/ECE6435/exp_schedule.html

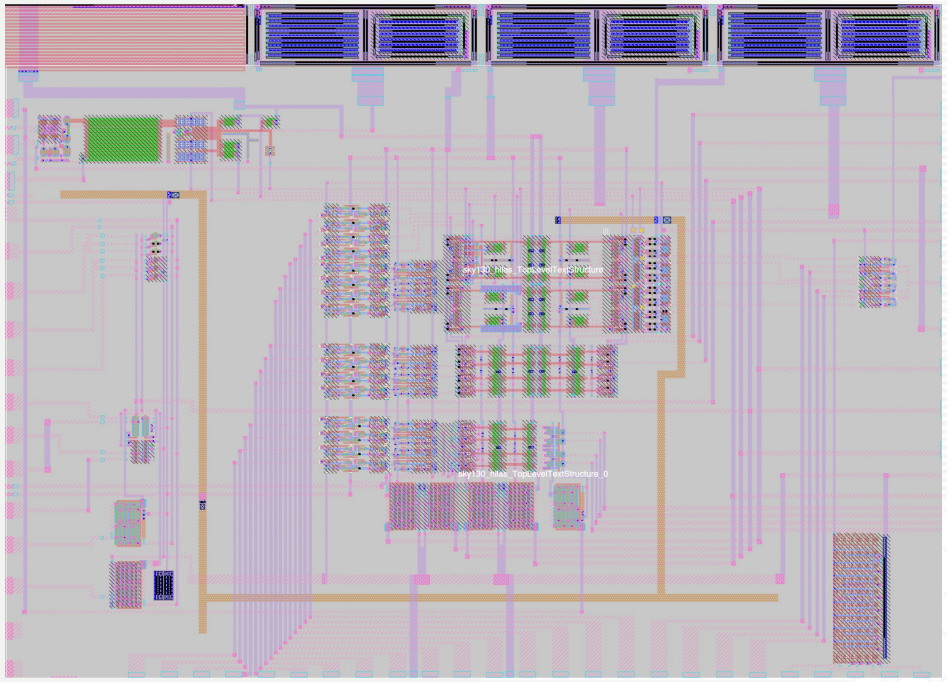




- J. Hasler, FPAA: History, Development, Classification: https://youtu.be/2lsz9gi8Oz8
- J. Hasler, Future of FPAA opportunities: https://youtu.be/rpSdb88ubfk
- J. Hasler & A. Natarajan, Intro Open-Source FPAA Toolset: https://www.youtube.com/8SVdhztVroc
- J. Hasler, Historical FG Perspective, https://youtu.be/R8iV01KZch4
- J. Hasler, FPAA Enabling Physical Computing, https://youtu.be/IGzinnykZIw

FPAA on-line Workshop: http://hasler.ece.gatech.edu/FPAAWorkshop/index.html





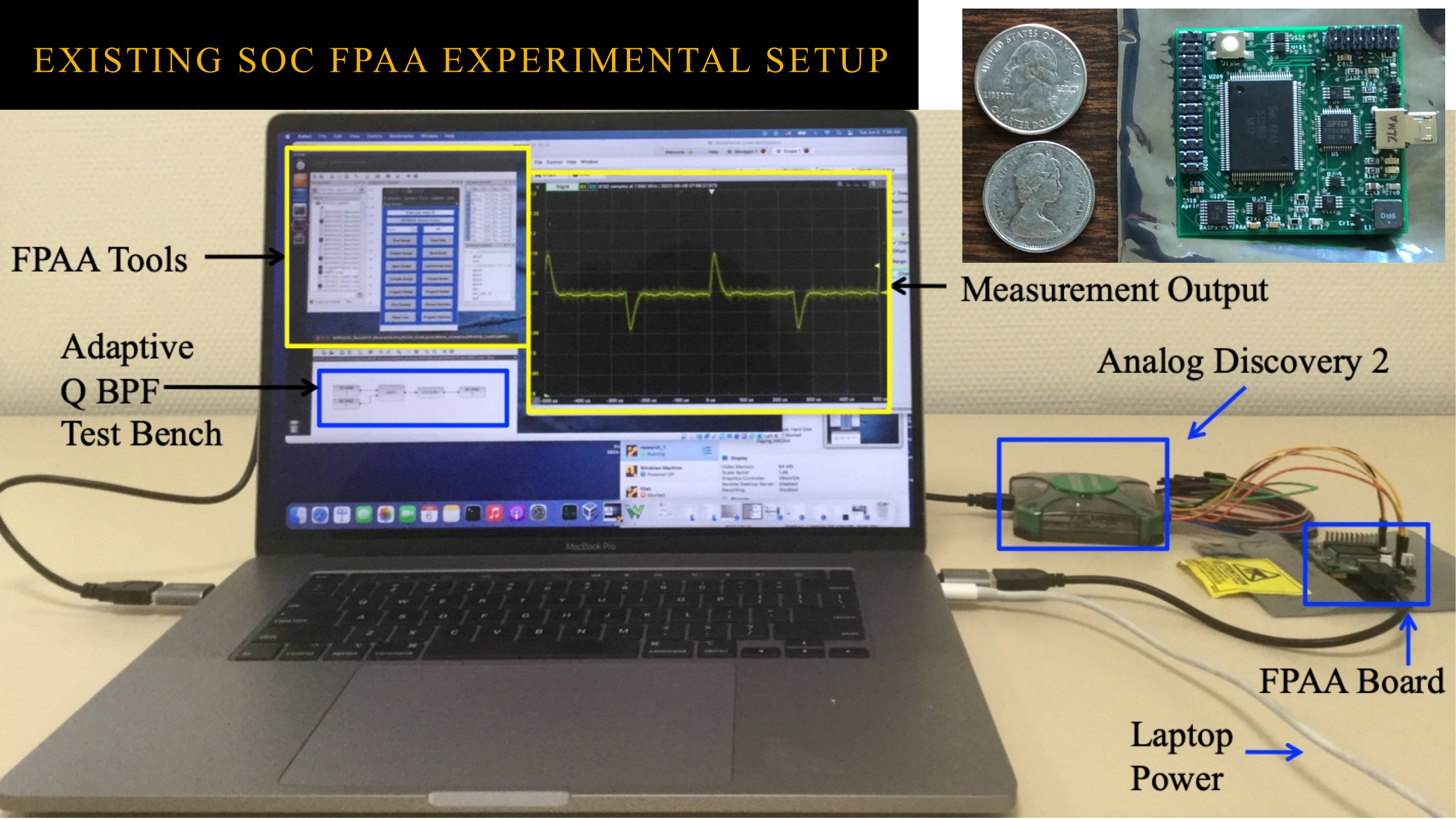
Okika: https://okikadevices.com

130nm Standard Cell

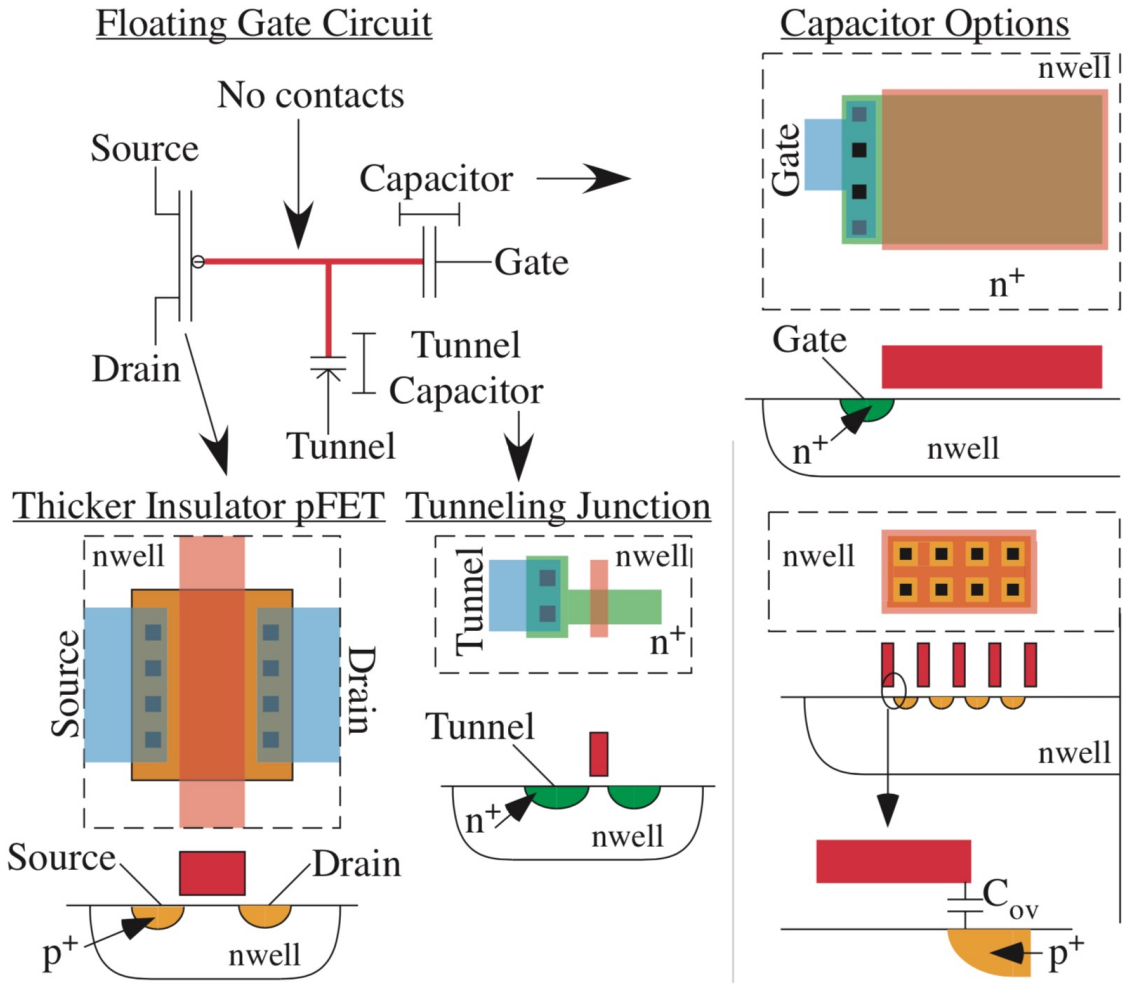
https://gitlab.com/um-ece/ftl-lab/hilas/designs/mpw2
https://gitlab.com/um-ece/ftl-lab/hilas/designs/alice.git

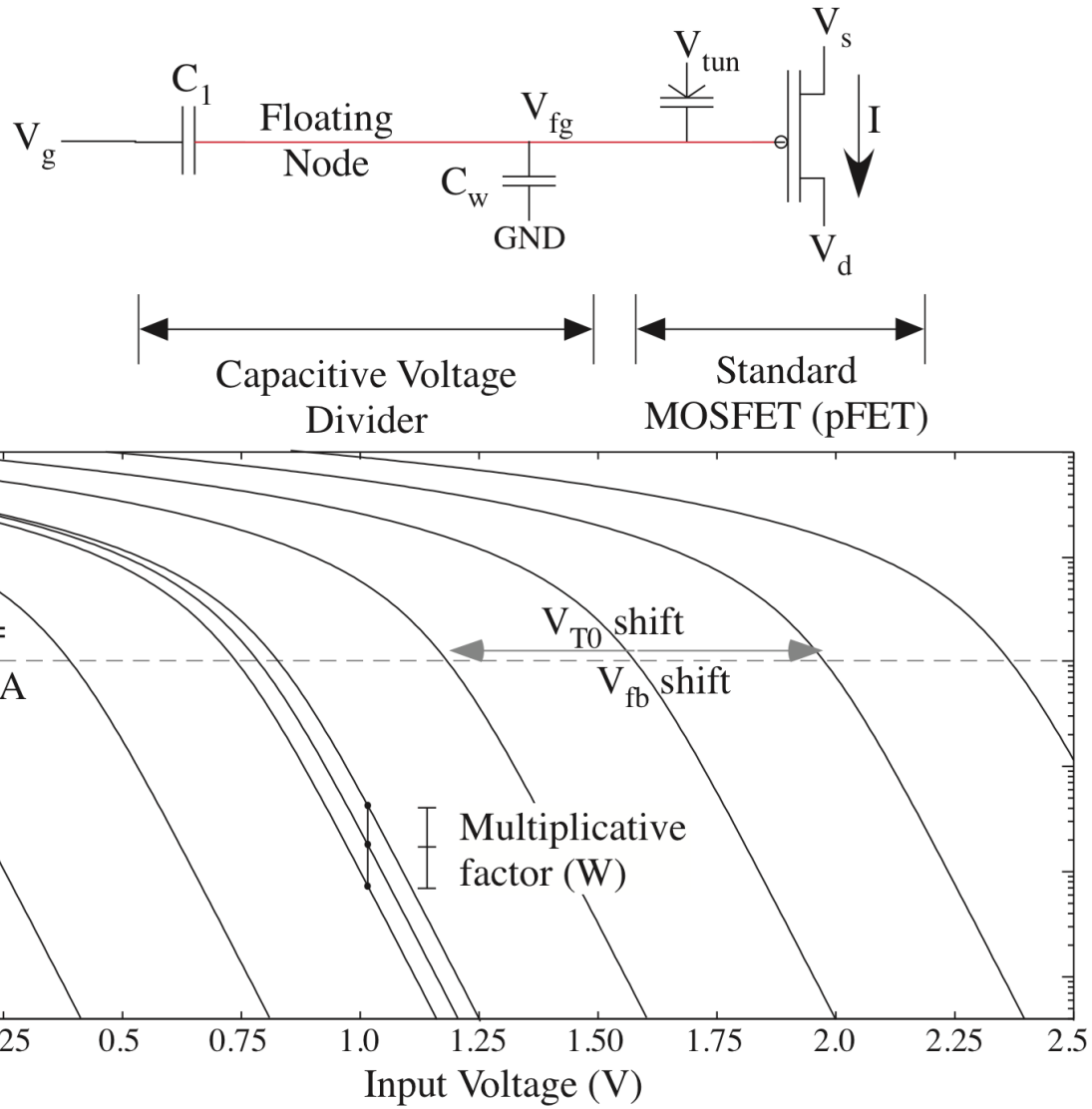
Synthesis tools: ASHES (1.5), https://github.com/a-folabi/ashes

EXISTING SOC FPAA EXPERIMENTAL SETUP



ANALOG PROGRAMMABILITY →FLOATING-GATE (FG) CIRCUITS



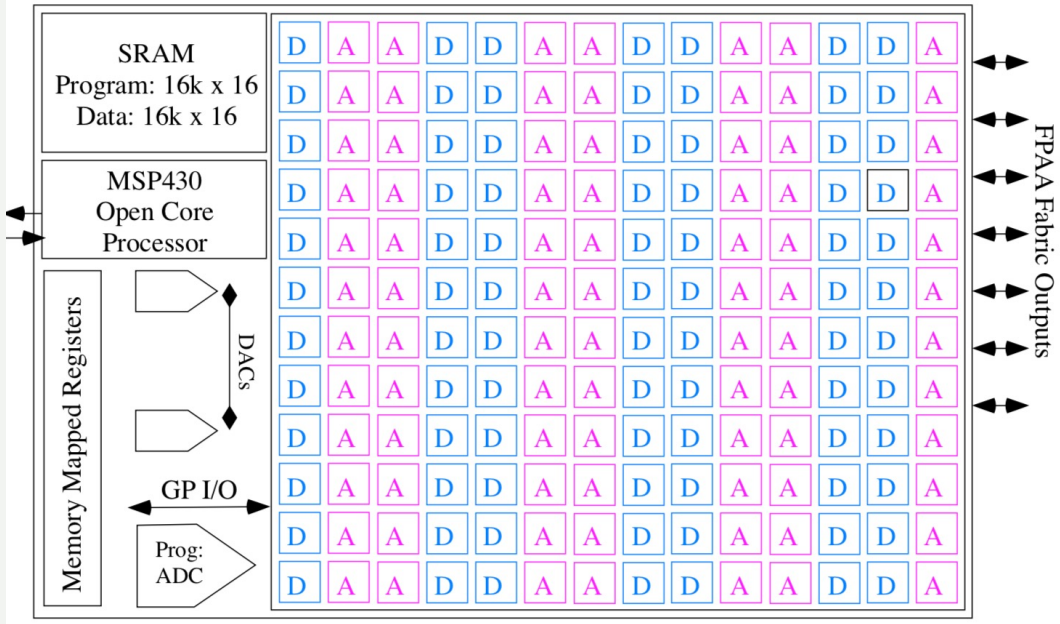


Program FG charge once and holds for part lifetime
(i.e. 10 year lifetime = 10-100μV)

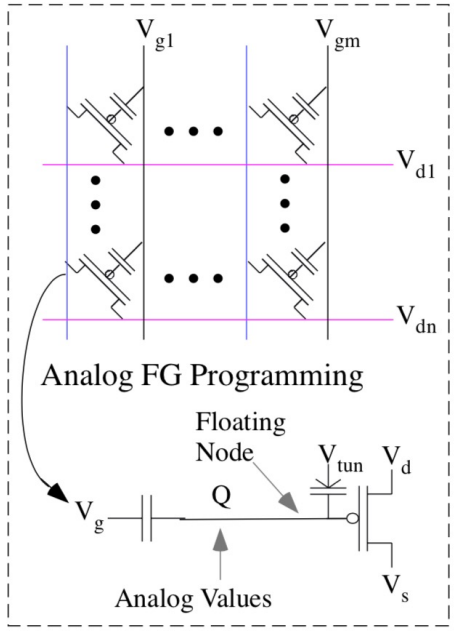
Programmed to 14bit accuracy: e.g. 60μV on 1V supply

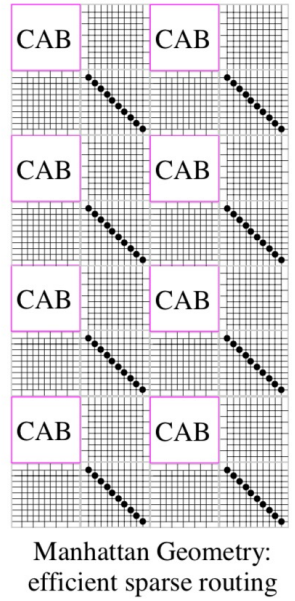
Floating-Gate (FG) circuit techniques enables direct solution for mismatch (V_{T0}) (Standard CMOS)

LARGE SCALE FIELD PROGRAMMABLE ANALOG ARRAYS (FPAA)

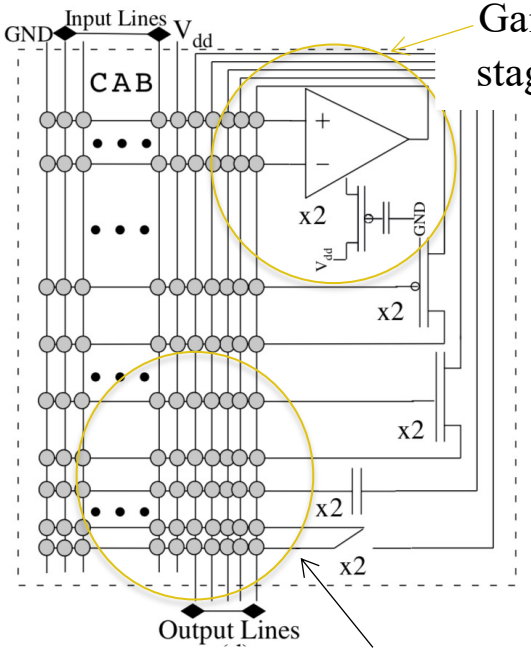


SoC FPAA:
350nm CMOS





Manhattan Geometry:
efficient sparse routing



Gain stage

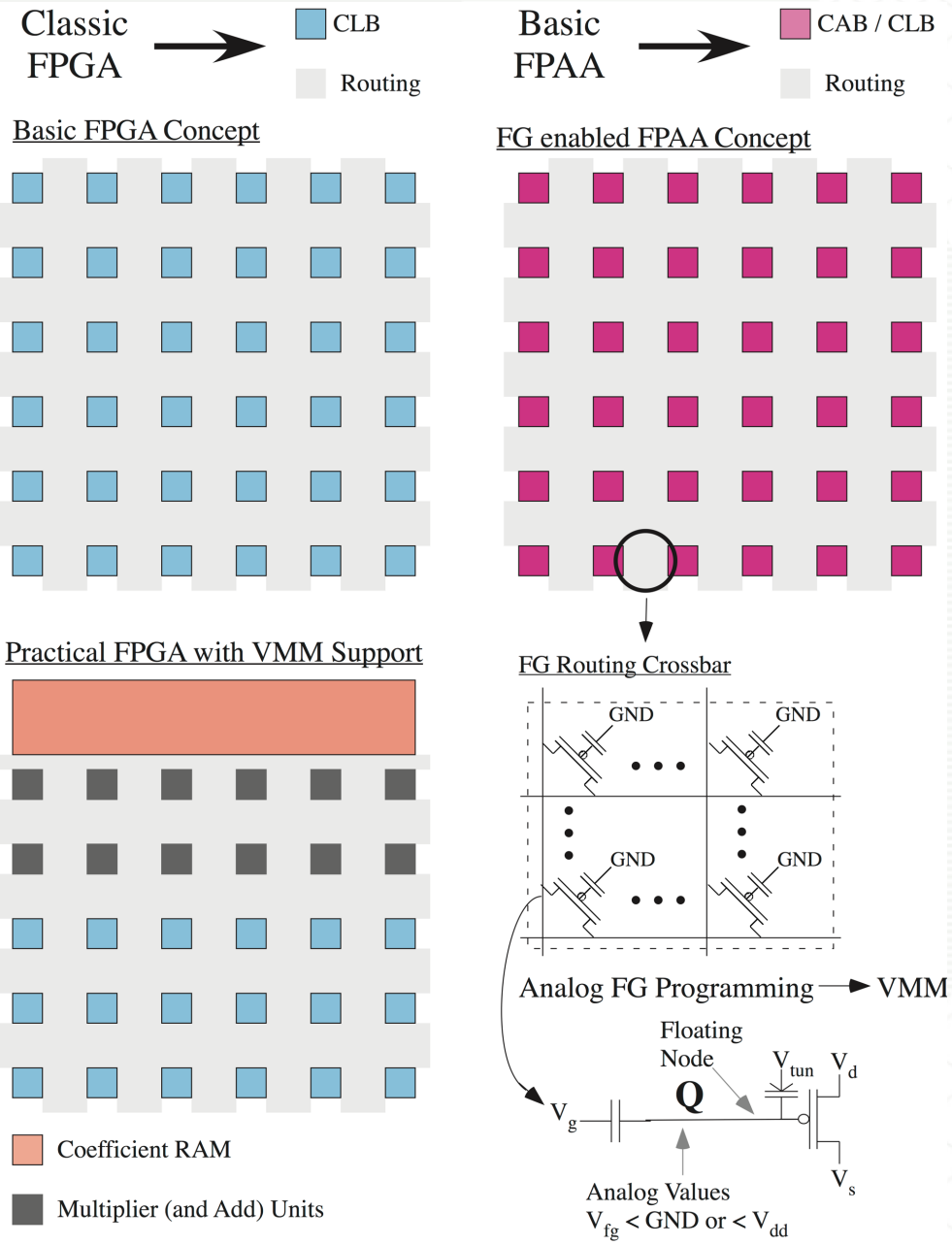
Switches =
FG crossbar

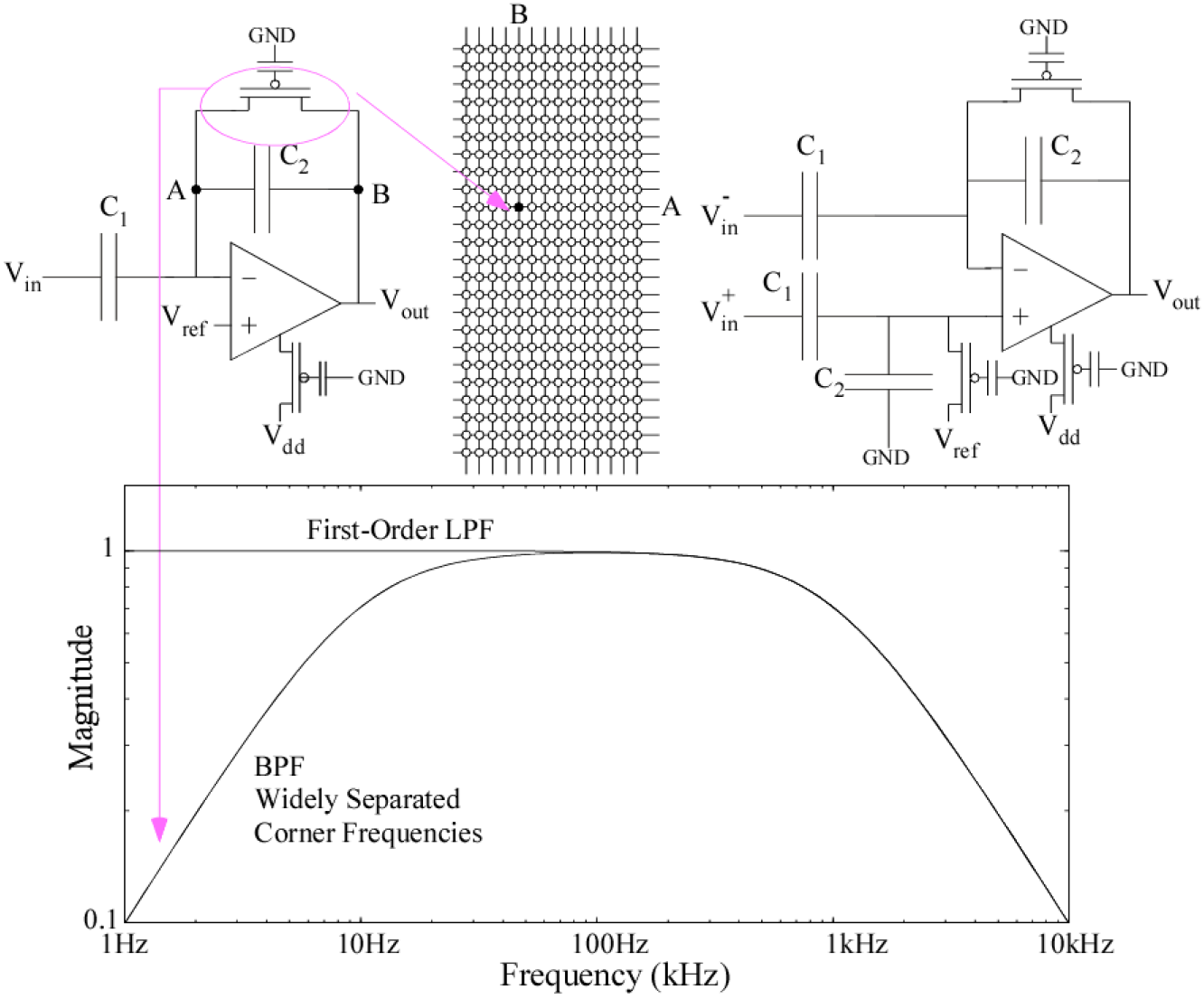
Partial List of Demonstrated FPAA Algorithms

Vector-Matrix Multiplication (VMM)	Analog Computing (e.g. ODE, Ax=b)	Embedded machine learning
Acoustic and Bio sensor processing	Neural interfacing and processing	Acoustic Inference and training
Optimal Path Planning	Neural architectures	Compressed Sensing Reconstruction
Delay lines and linear phase filters	Spatiotemporal Beamforming	IC security / Noise Generators

"Switches are not Dead Weight" (2007)

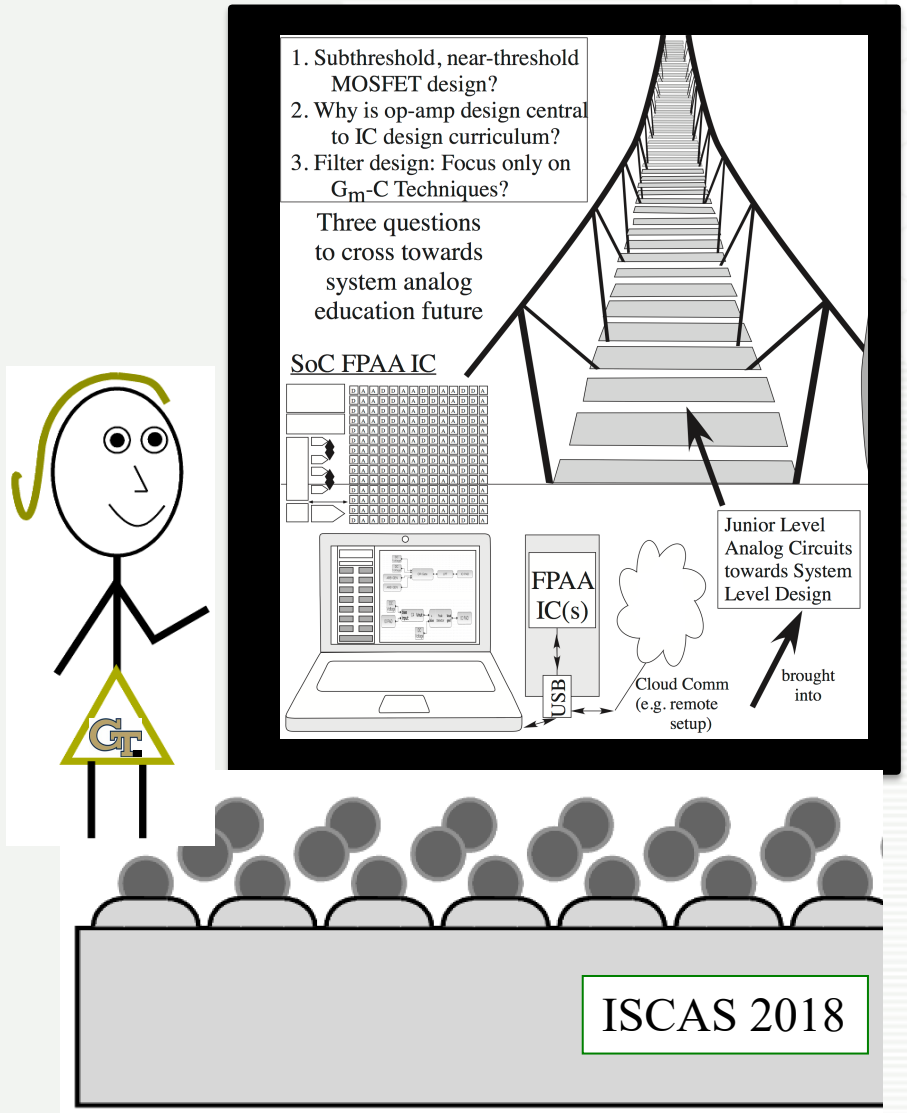
FPAA ROUTING → COMPUTATION





- Vector-Matrix Multiplication
- Current / Voltage Sources
- Synaptic arrays

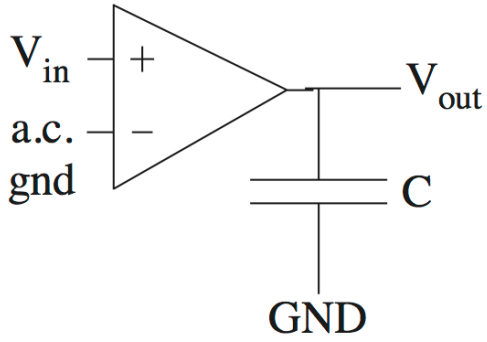
- Passive Dendrites
- Resistive Networks
- and more….



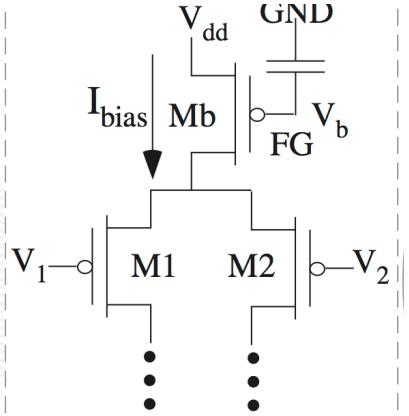
Transconductance-C design

Advantages:

1. Highest bandwidth for given energy
2. Lowest Noise for given I_{bias}

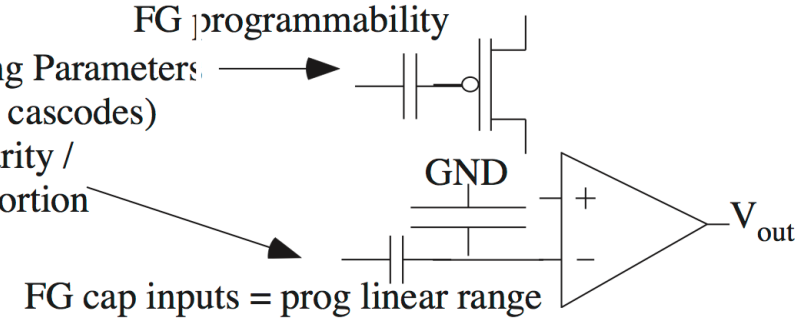


Needs Programmability & Linearity & Offset compensation



Issues:

1. Setting Parameters (bias, cascodes)
2. Linearity / Distortion



Abstract Analog Circuits

Prog accuracy not by feedback

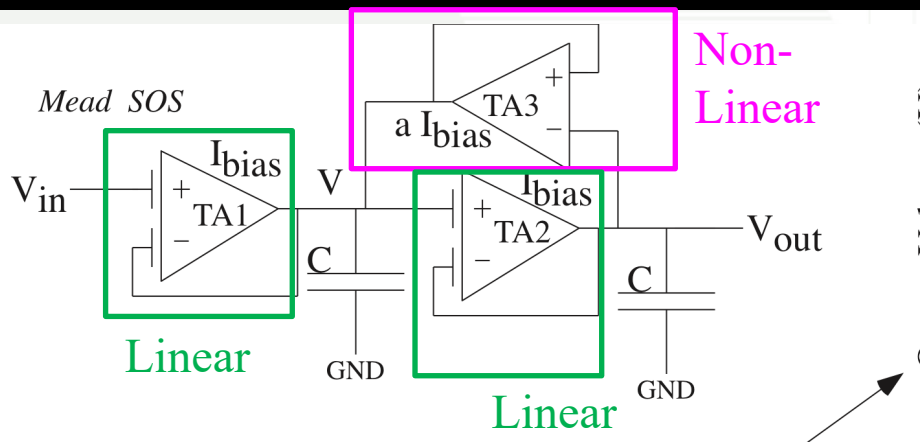
IC design transformed by programmability →

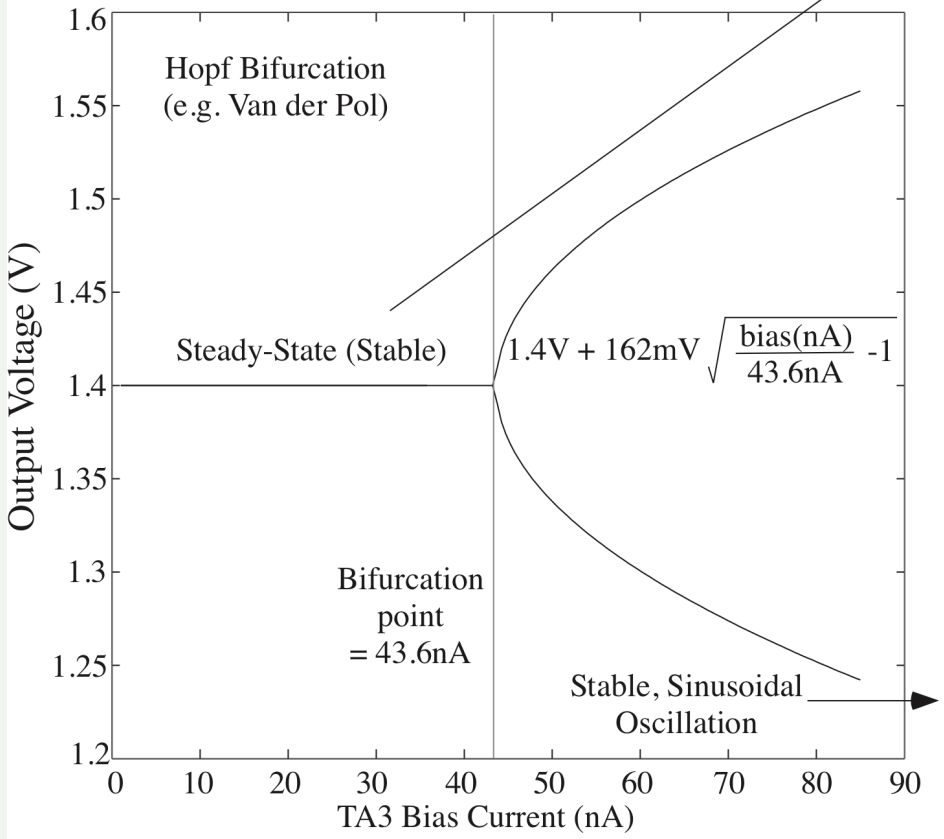
- Prog. FG biasing
- FG TA inputs
- GmC, SubV_T Design (**no bank of passives**)
- Configurable Design

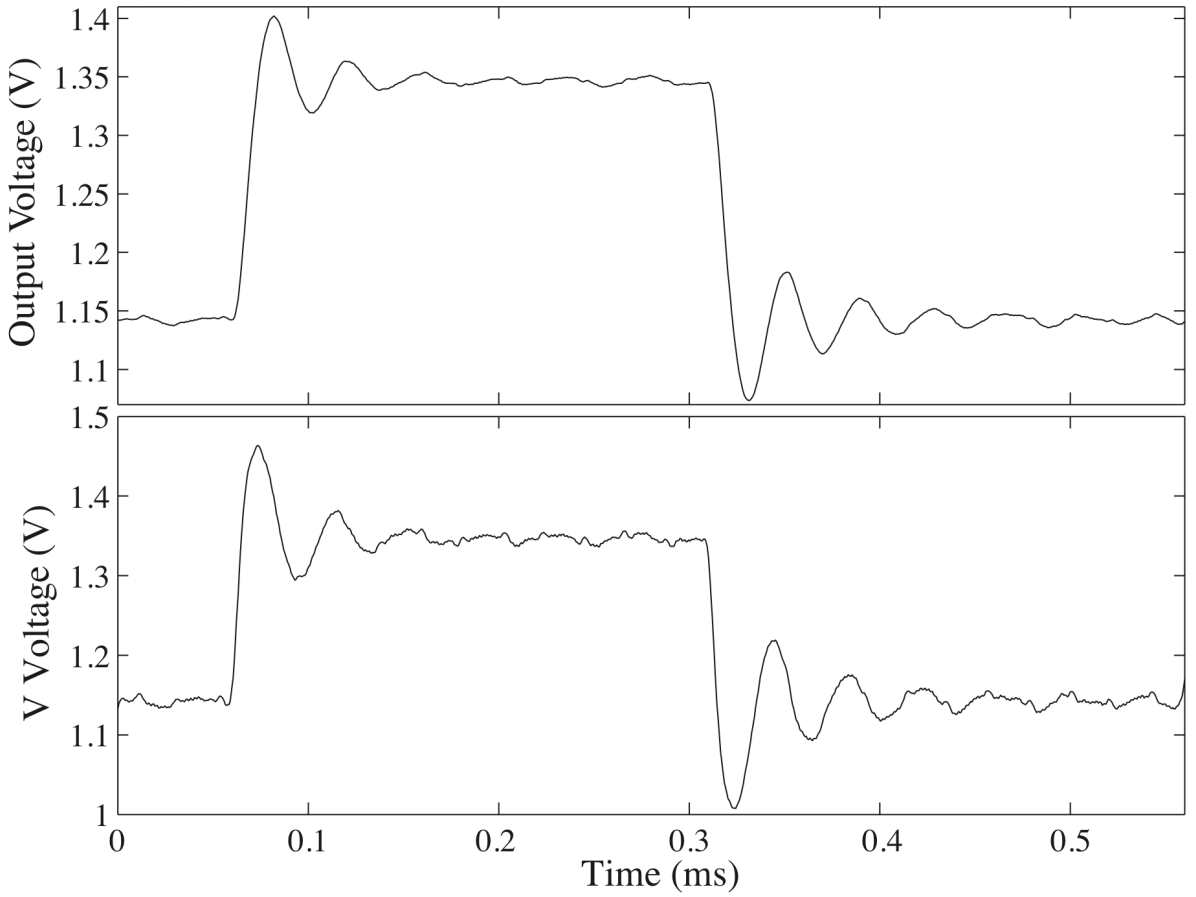
Transistor Centric Design → Few (to 0) passives other than capacitors

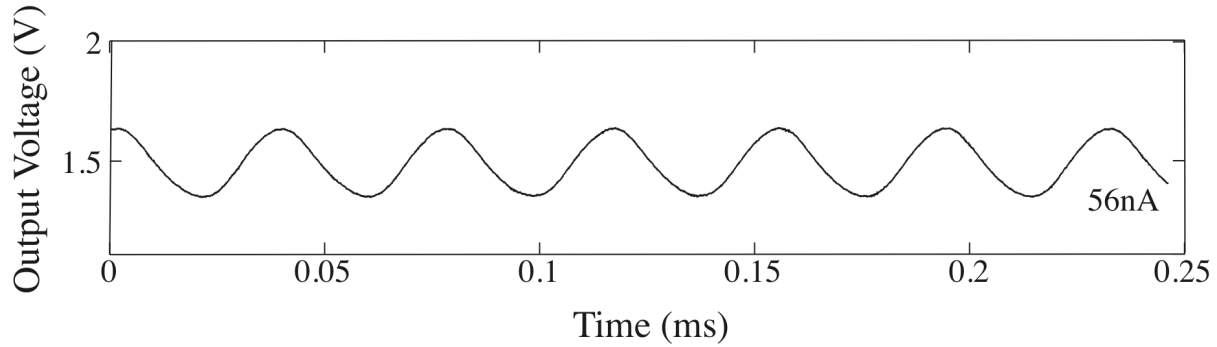
Subthreshold Centric Design → Wide tuning range, low-power / energy

PROG HOPF BIFURCATION CIRCUIT (FPAA)

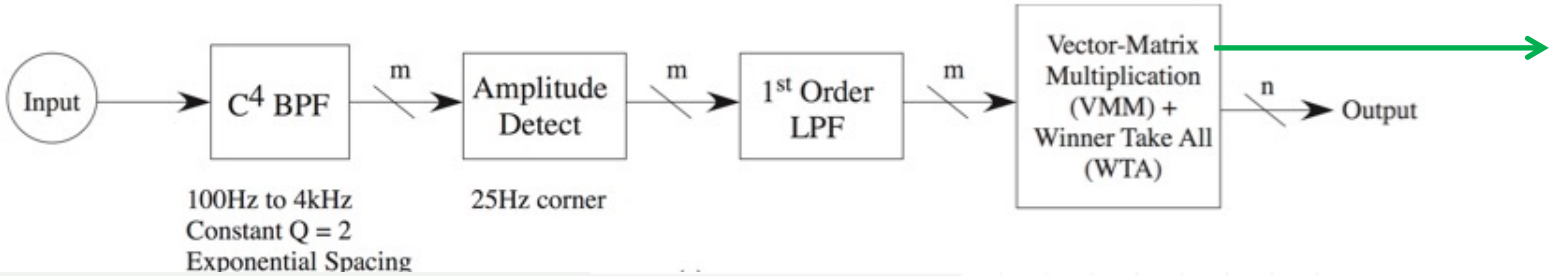






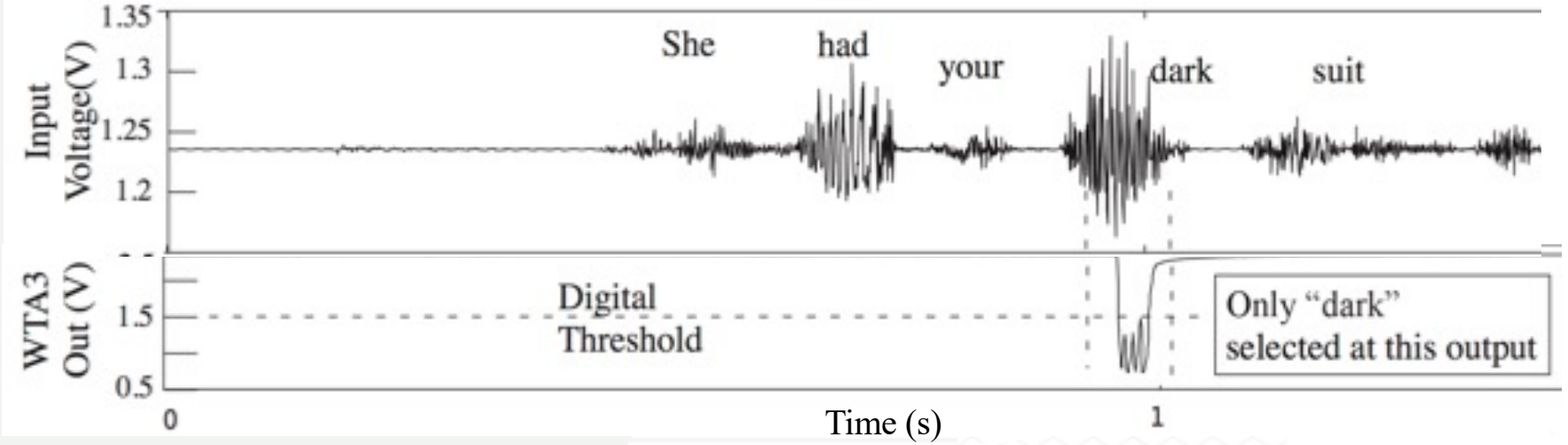


FPAA Acoustic Classification



Single Layer VMM+WTA
= universal approximator

Recognizing the word "Dark" (TIMIT): Command Word Recognition (2016)

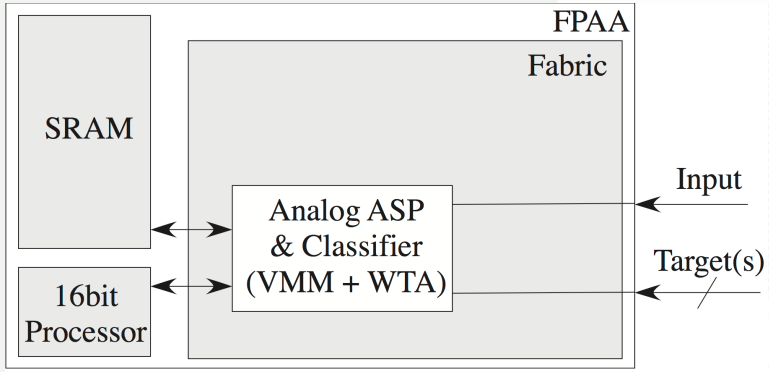


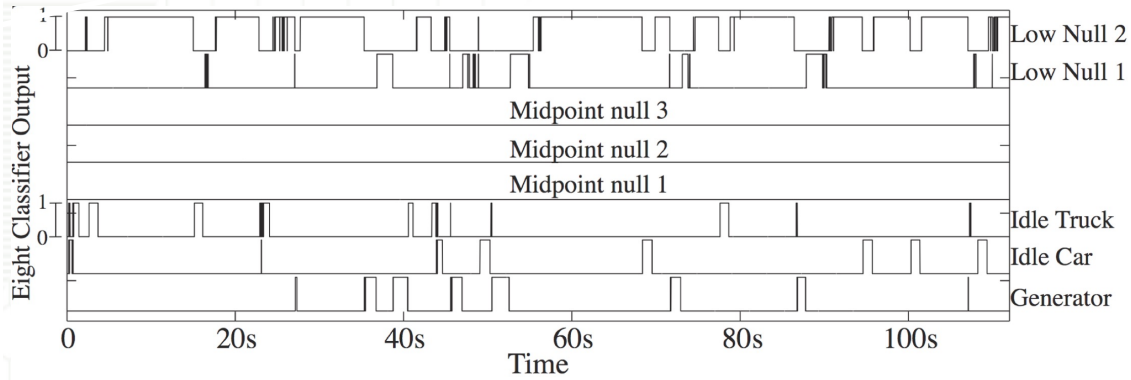
Embedded learning & classification:20-30µW

Demonstrates 1000x Energy Efficiency, 100x Area Efficiency

< 23µW power

Classification +- On-Line Training

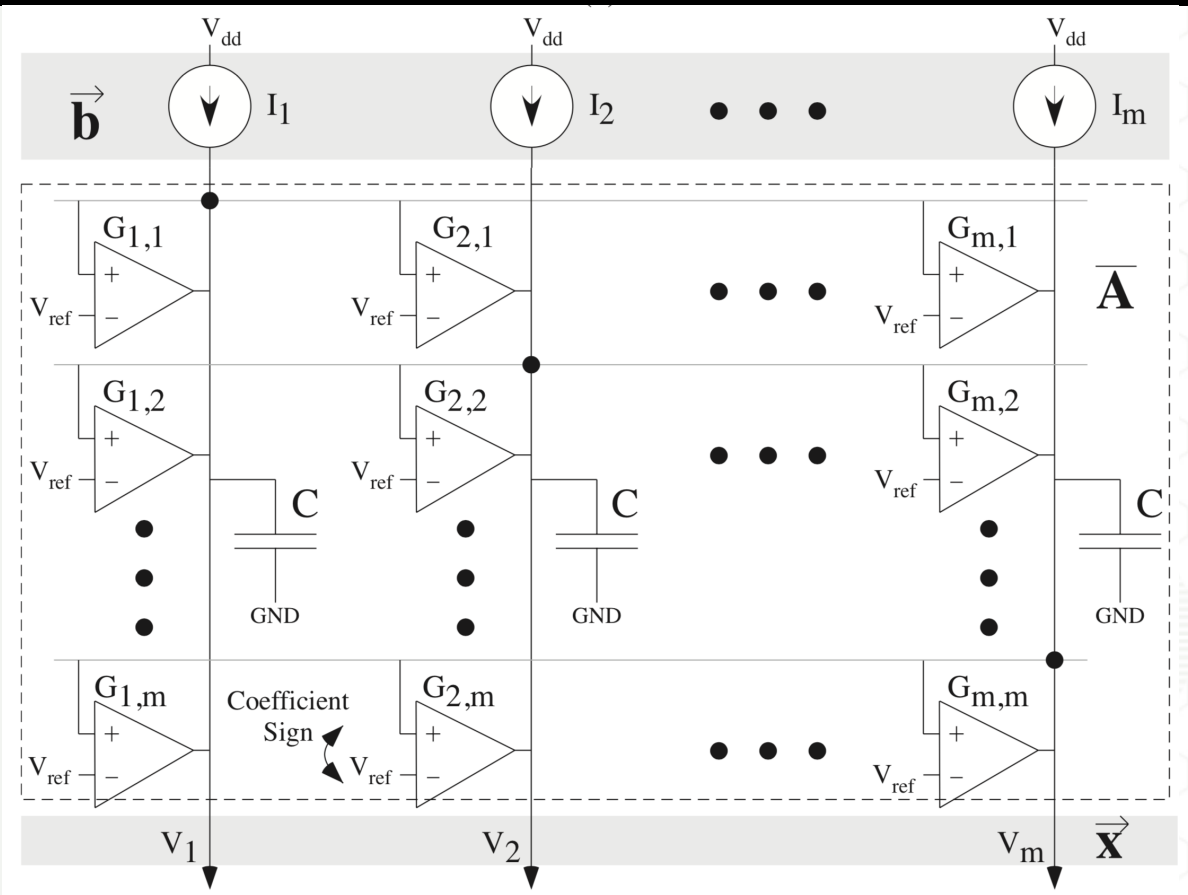




100% classification

[GOMAC 2016, ECAS 2018]

FPAA Solving Linear Equations

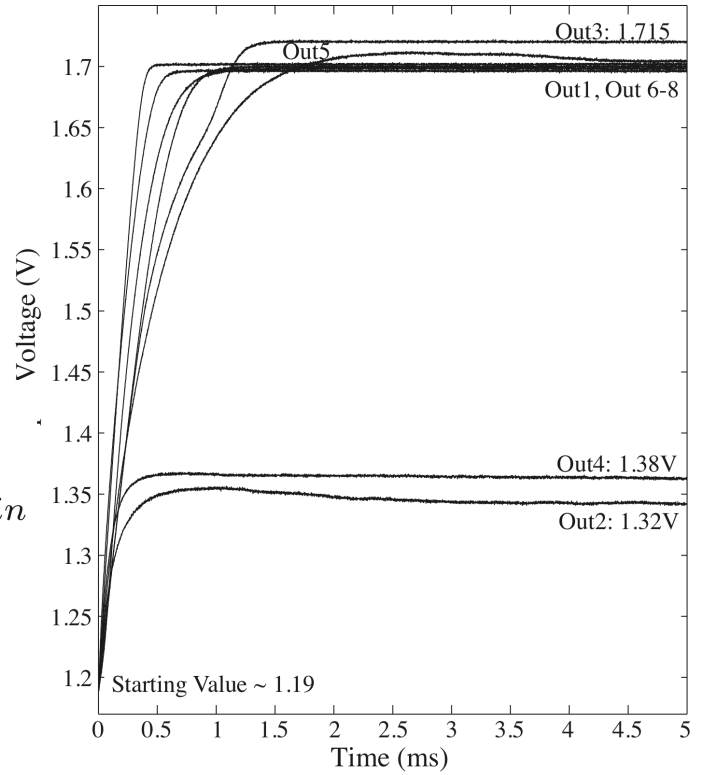


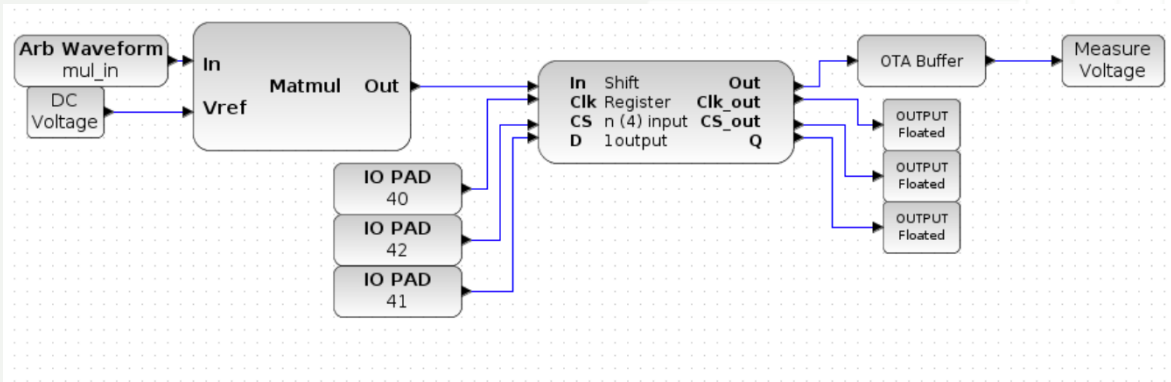
$$C\frac{dV_l}{dt} = I_l - \sum_{k=1}^{m} G_{l,k}V_k$$

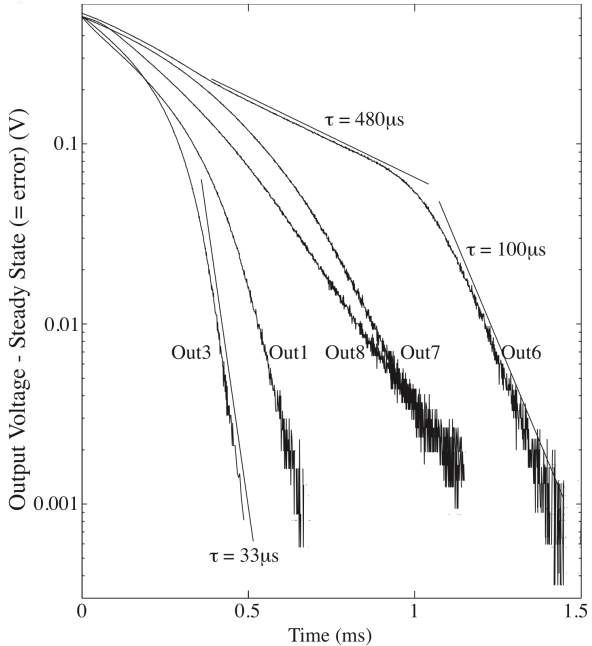
$$a_{l,k} = G_{l,k}/G_{min}$$

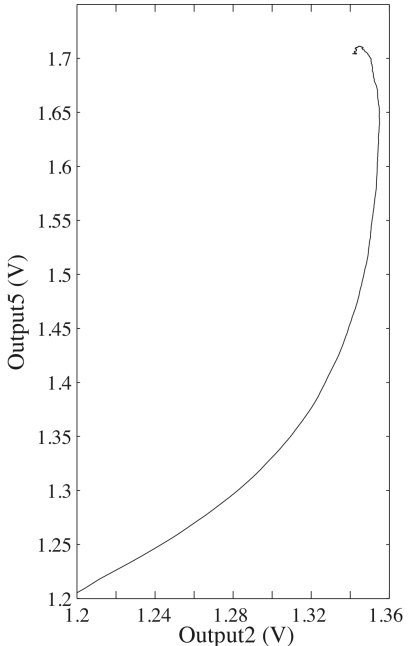
$$b_k = I_k/G_{min}, \tau = C/G_{min}$$

$$\tau\frac{d\mathbf{x}}{dt} + \mathbf{Ax} = \mathbf{b}$$

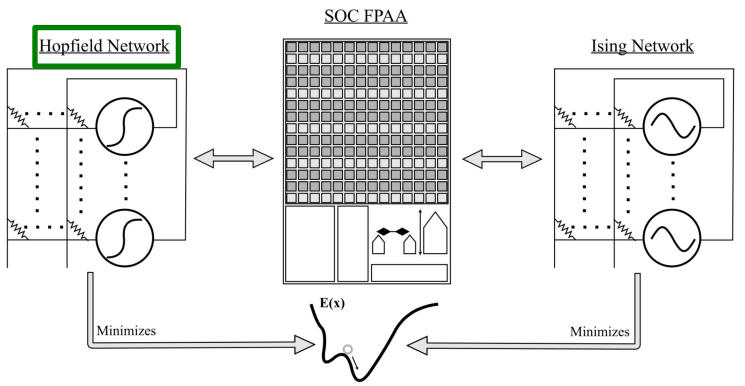


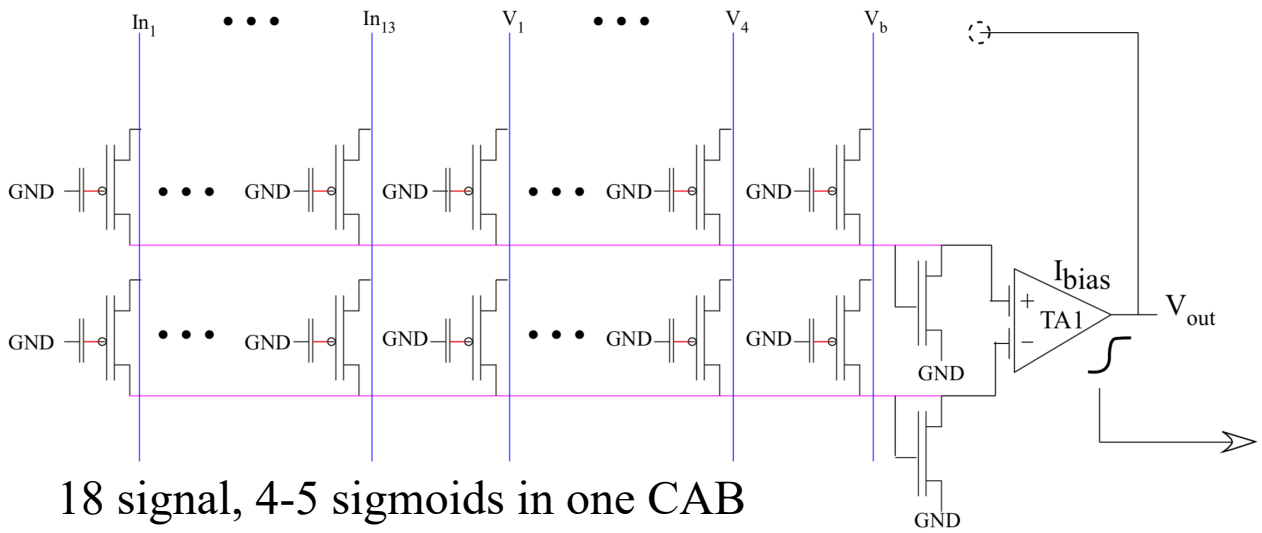






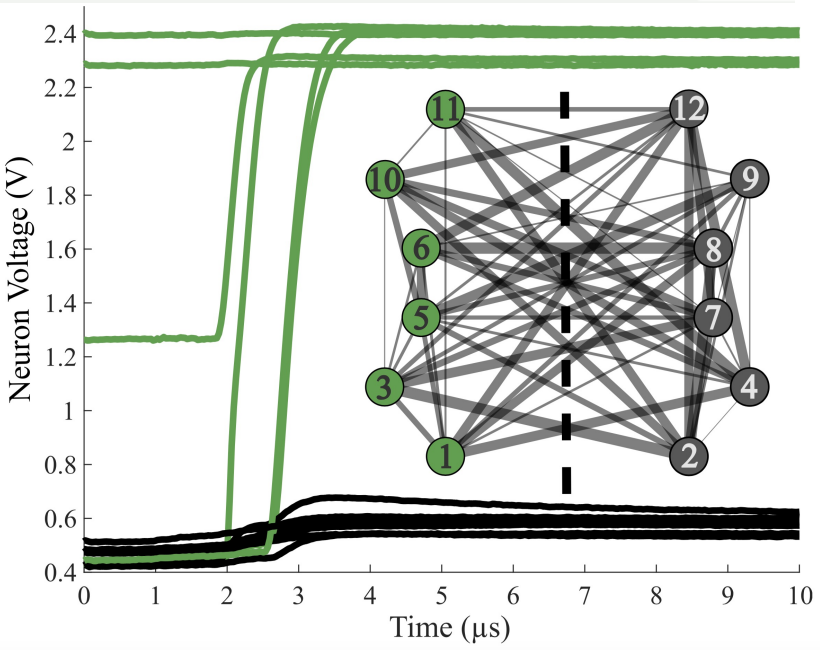
FPAA Hopfield Networks



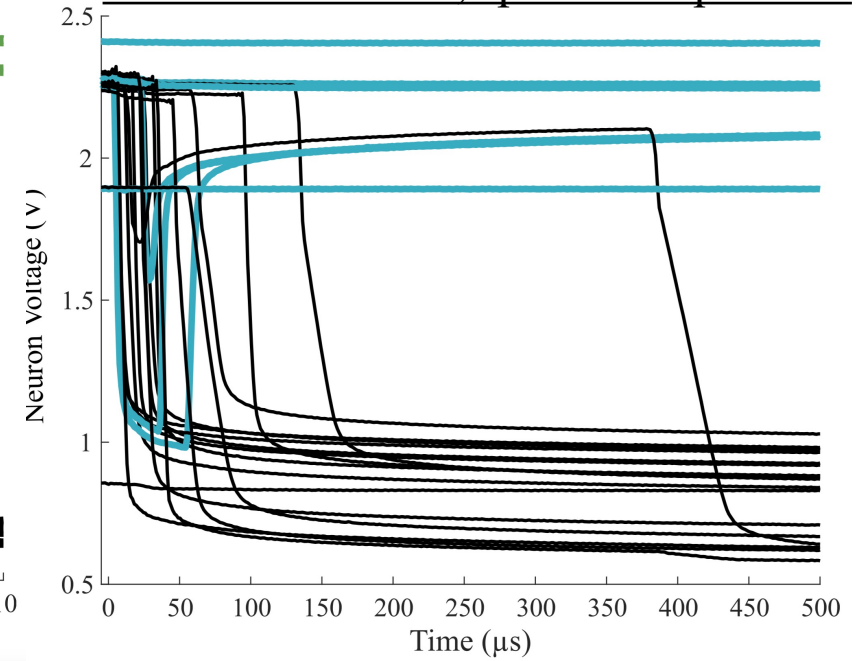


18 signal, 4-5 sigmoids in one CAB

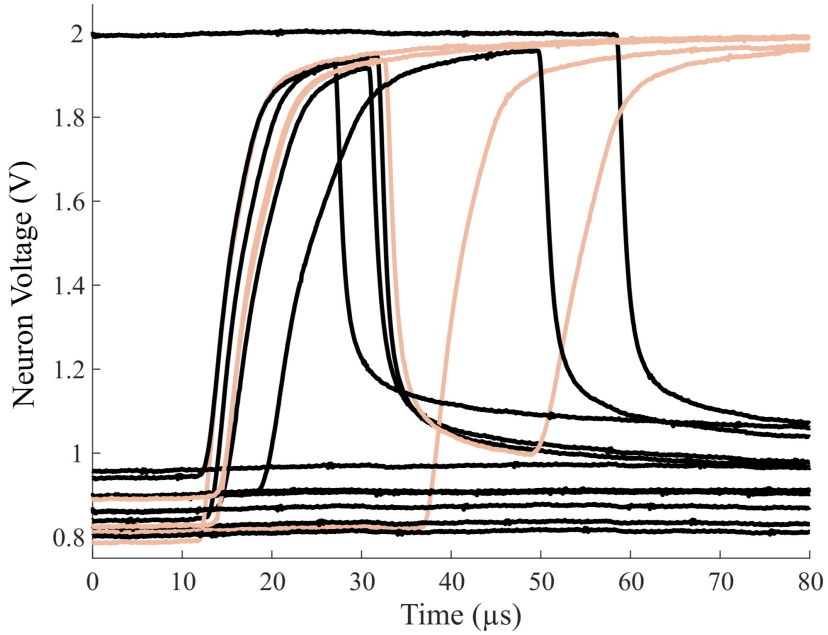
12 Variable Max Cut (analog weights)



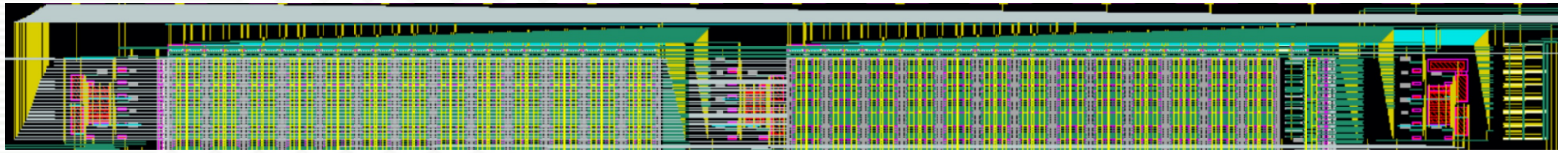
24 Variable 3-SAT, sparse computation



4 city TSP (16 node network)

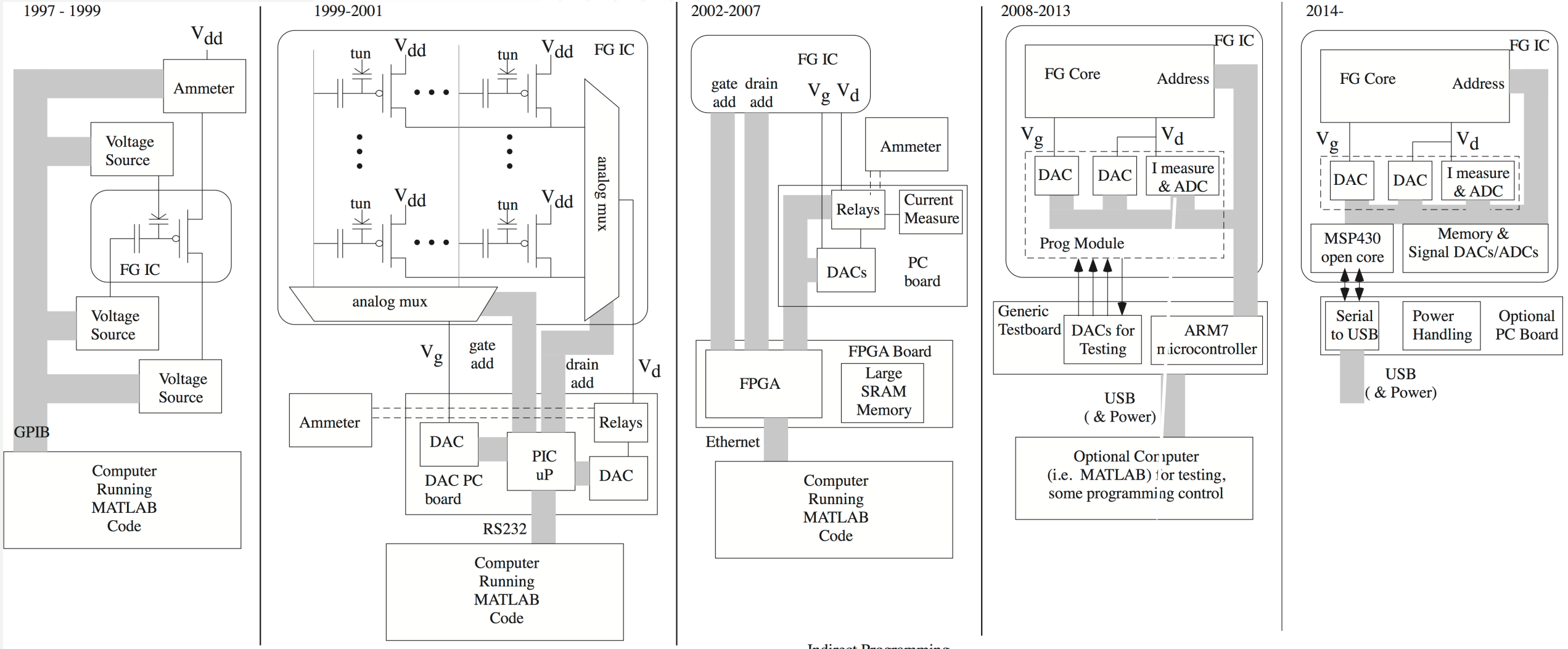


65nm CMOS Hopfield
(25x25 & 25x25 input)



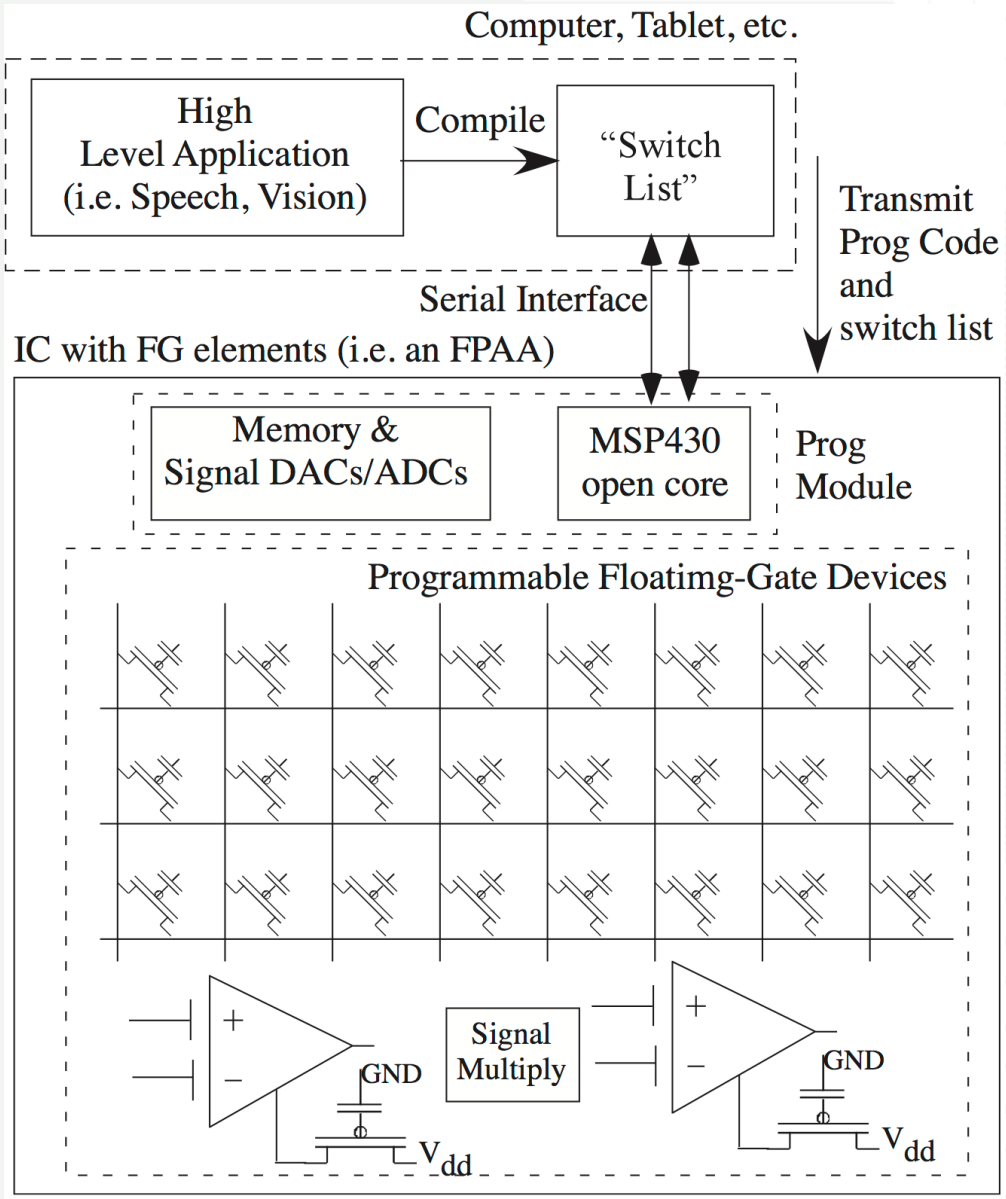
0.5mm x
0.05mm

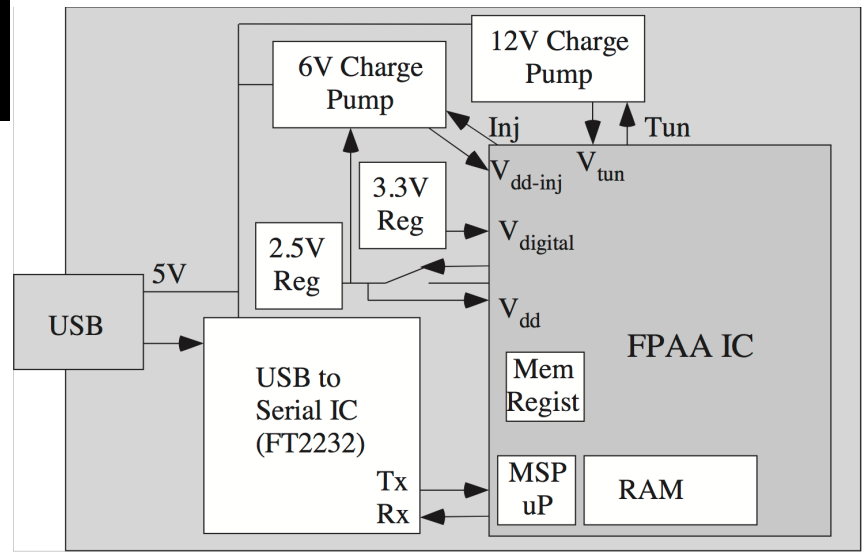
GT FG PROGRAMMING HISTORY



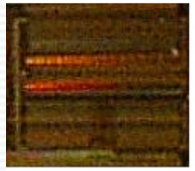
GT FG PROGRAMMING ARCHITECTURES

FPAA FG Programming Approach

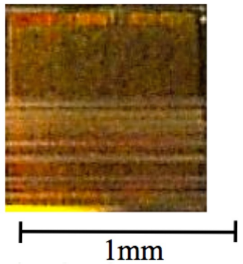




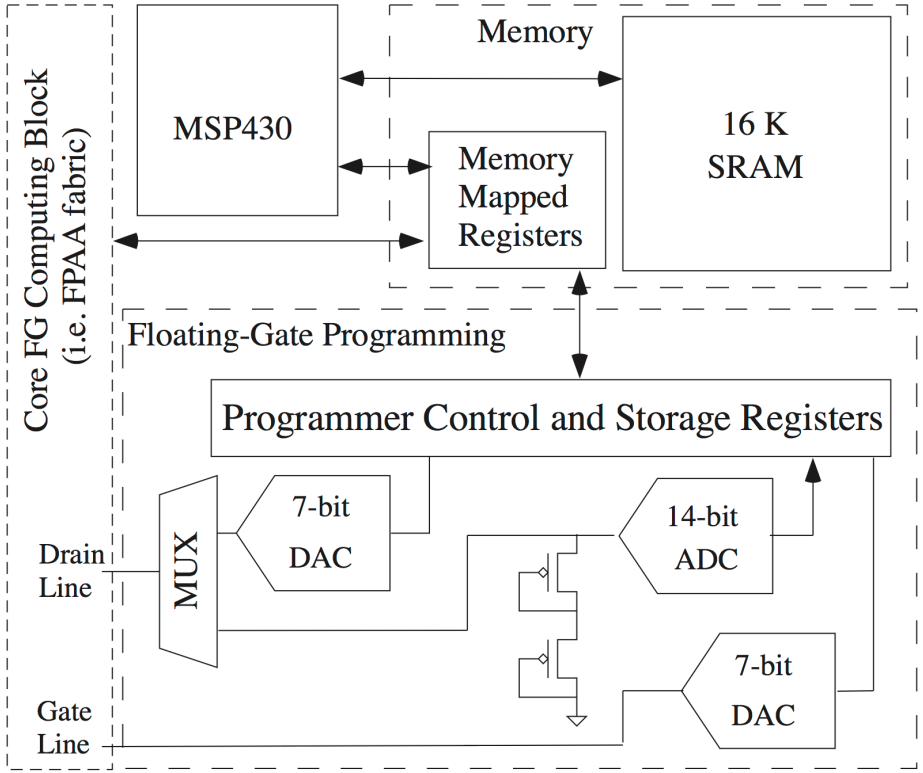
Programmer (0.75mm x 0.92mm)



uP (0.92mm x 0.92mm)

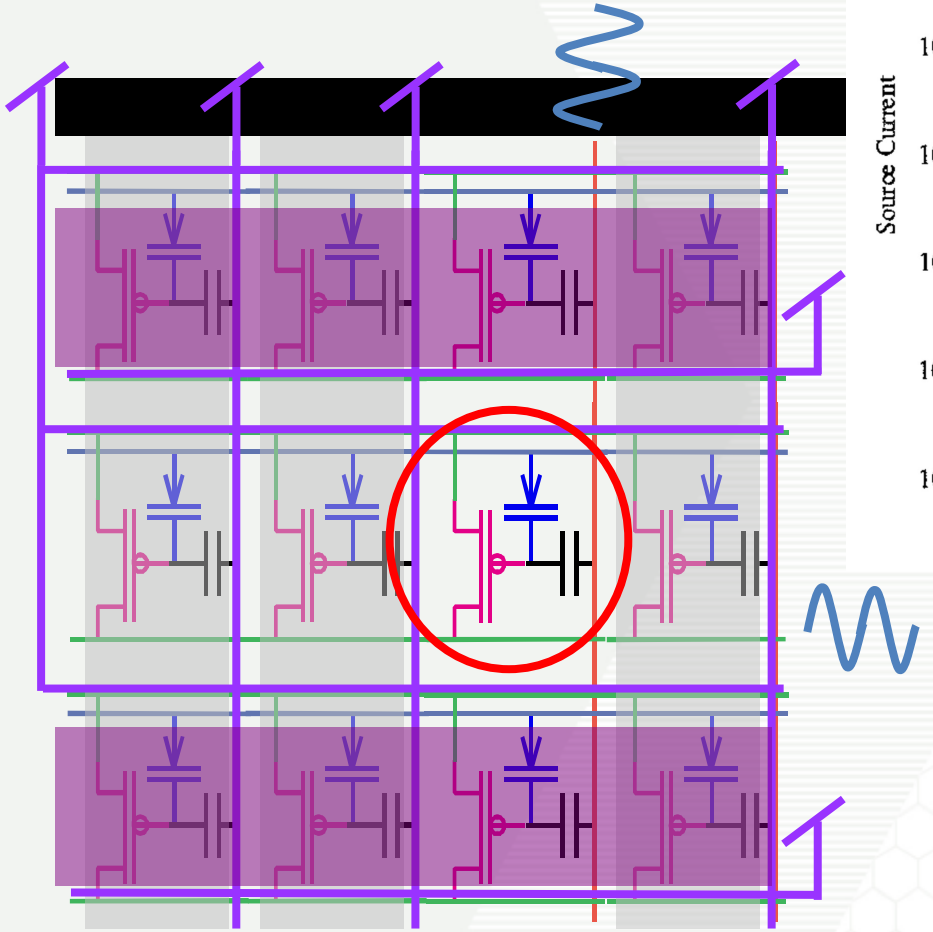


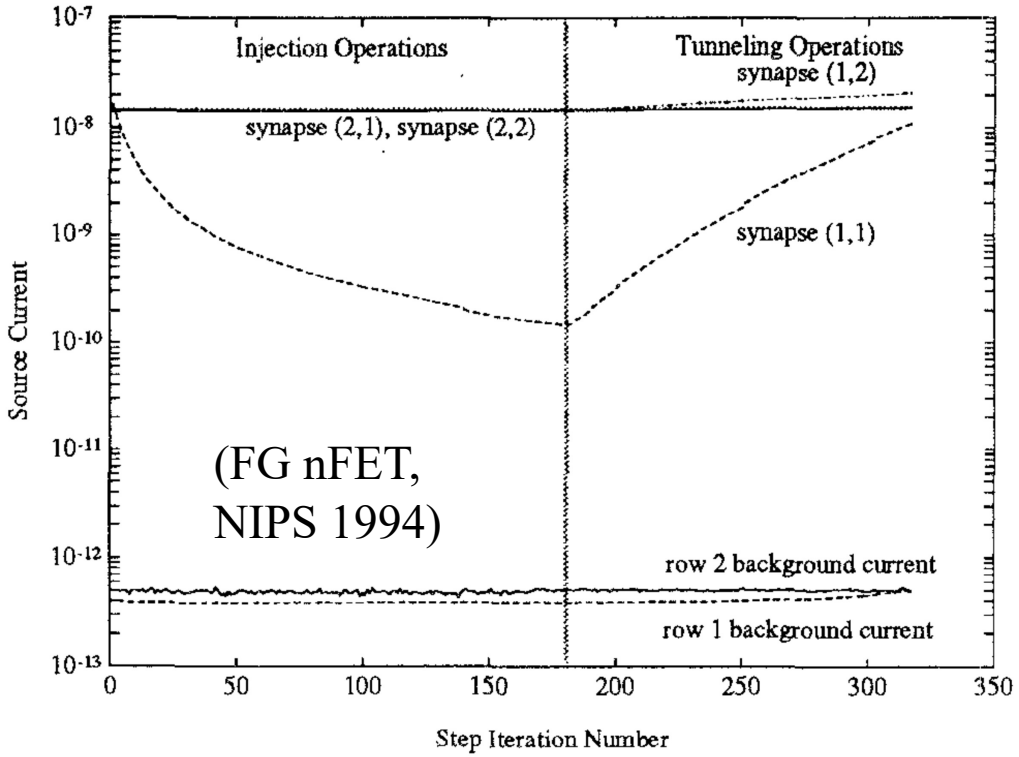
SRAM (1.5mm x 3.5mm)



FG SELECTIVITY IN 2D ARRAY

Isolation of single FG Device
in a 2D array

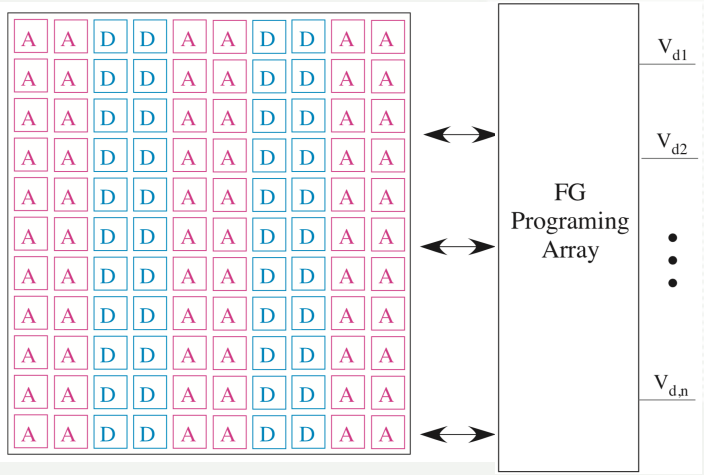




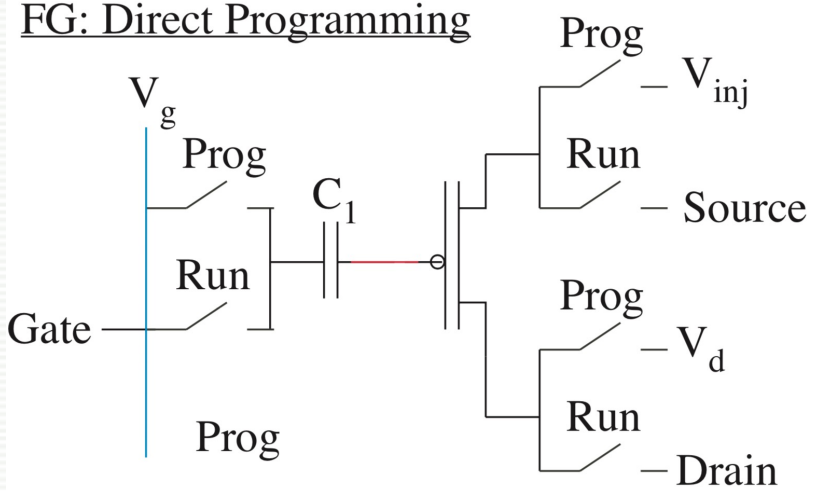
Hot-Electron Injection: ~0
disturb for array devices

Electron tunneling: row disturbs
Tunneling ~ strongest nonlinearity
(any other device is worse)

DIRECT VS. INDIRECT PROGRAMMING

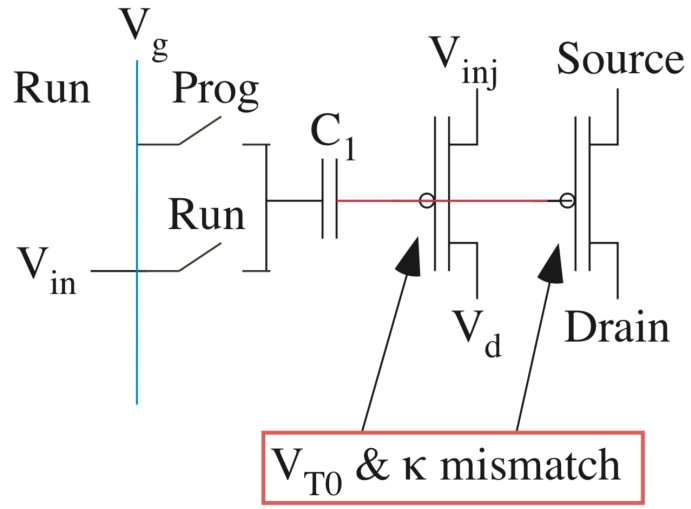


FG: Direct Programming



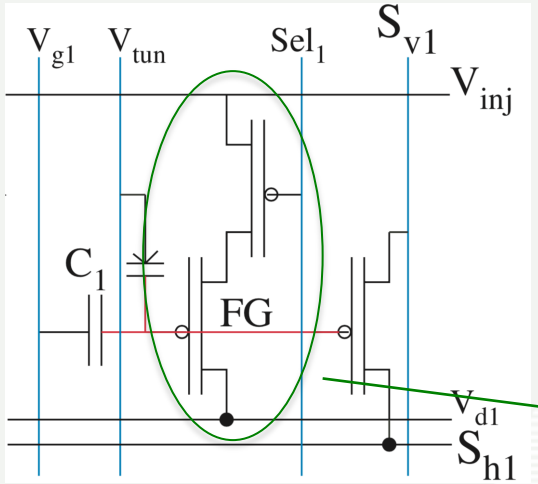
- More switches & in signal path
- No Mismatch from programmed value

FG: Indirect Programming



- Fewer Switches

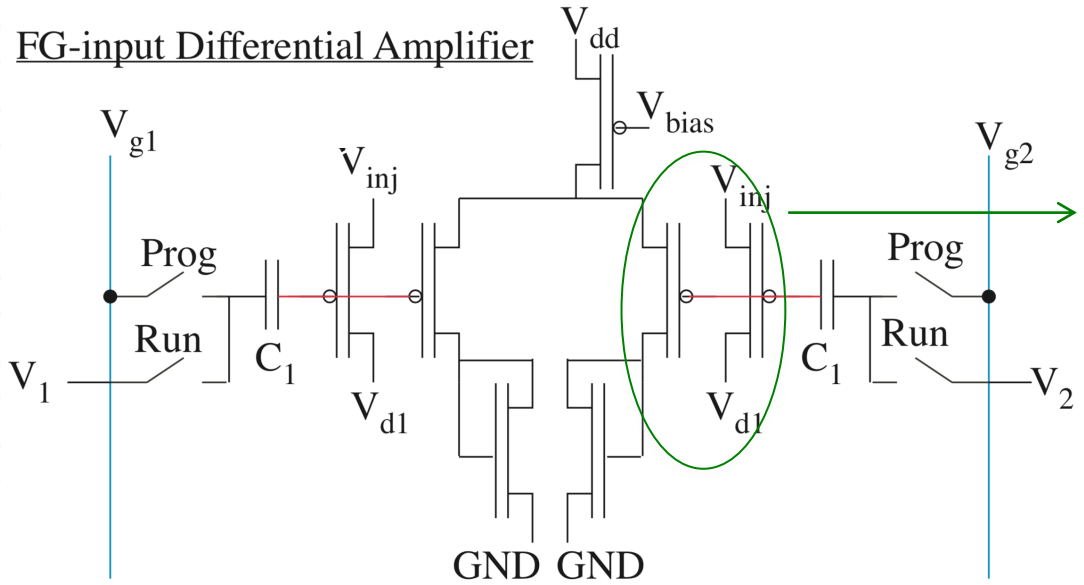
Switch with Wide Current Range



Programming pFET with shutoff pFET to enable perfect selectivity without affecting the crossbar switch

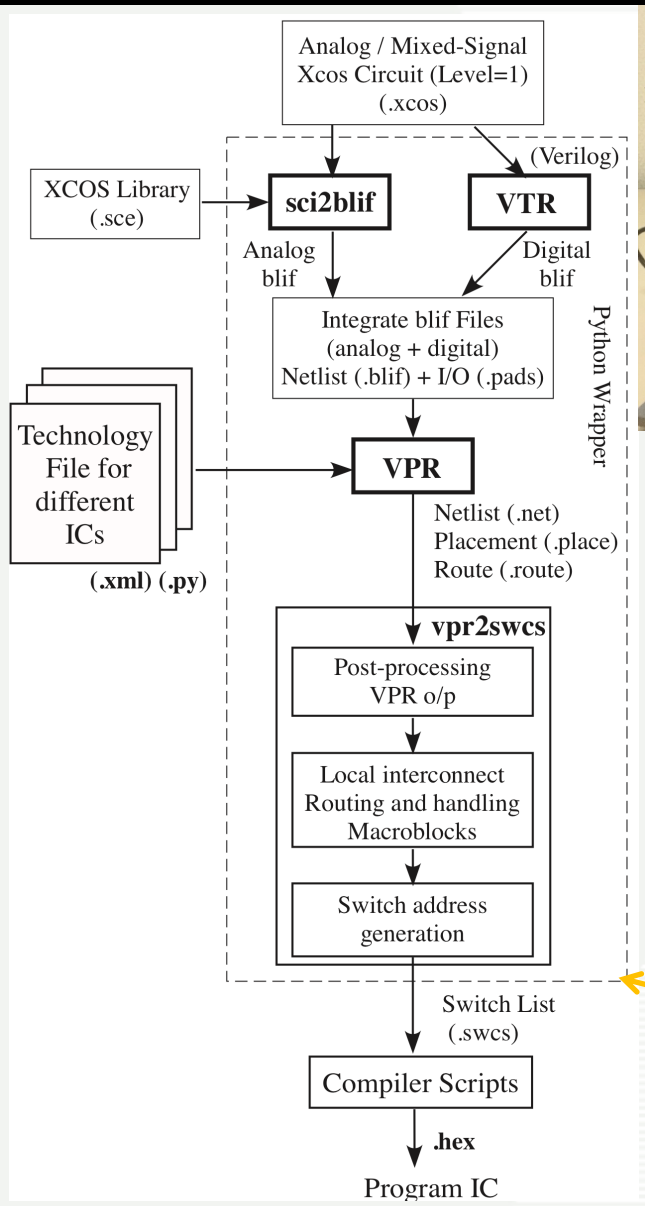
Today's SoC: Used for most switch elements

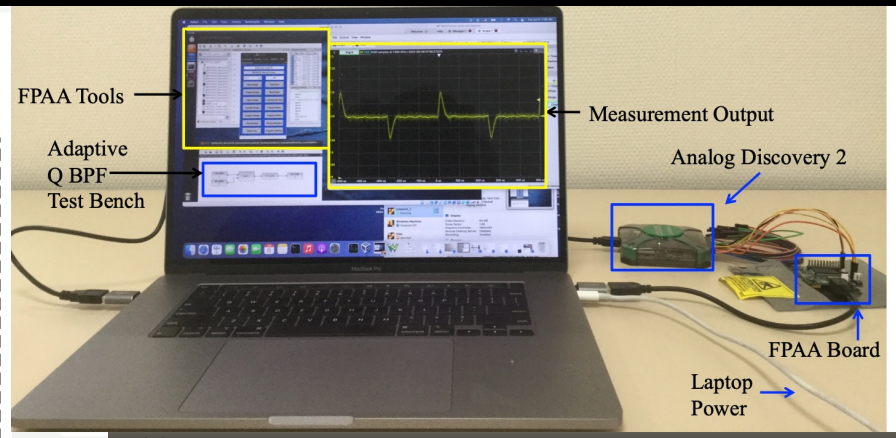
FG-input Differential Amplifier

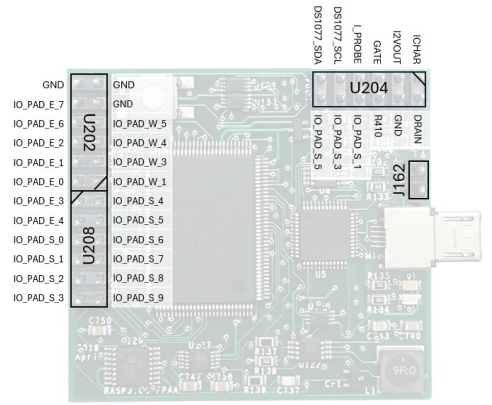


No switches in the I signal path, only gate input voltages

FPAA TOOL FRAMEWORK

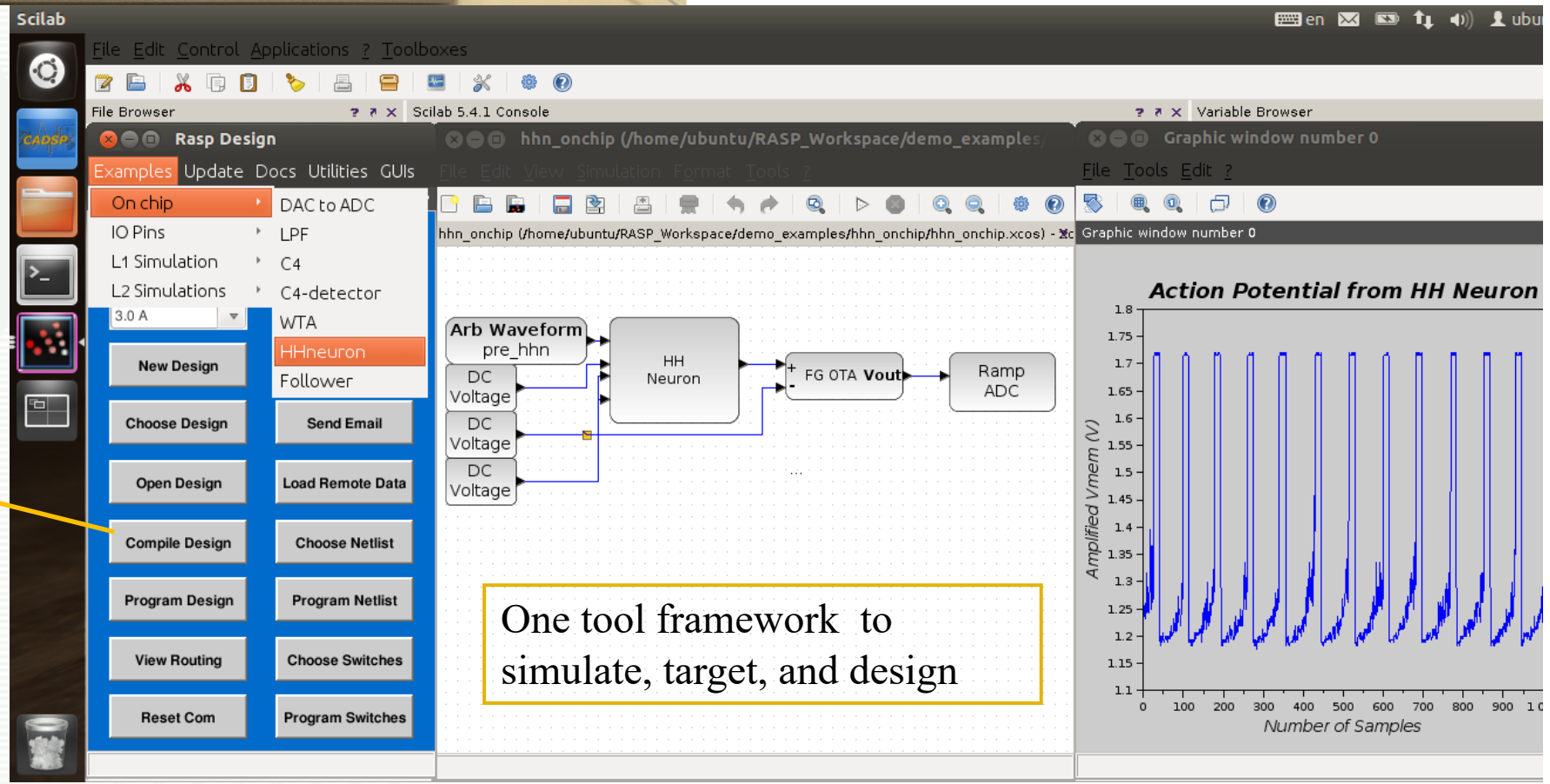






Design
→Hardware
→ Simulation

Used in classes
> 10 years



NEXT GENERATION ANALOG TOOLS & TARGETING FPAAS & PROGRAMMABLE ANALOG STANDARD CELLS

Analog & Mixed-Signal Standard Cells

65nm CMOS

350nm CMOS

28nm CMOS

Skywater

130nm CMOS

180nm CMOS

16nm CMOS

[CAS I, Hasler, et. al, 2024]
[CICC, Mathews, et. al, 2024]
[ESSERC, Ayyappan 2025]

HLS Application specification

Lowering

Algorithms

Lowering & PnR

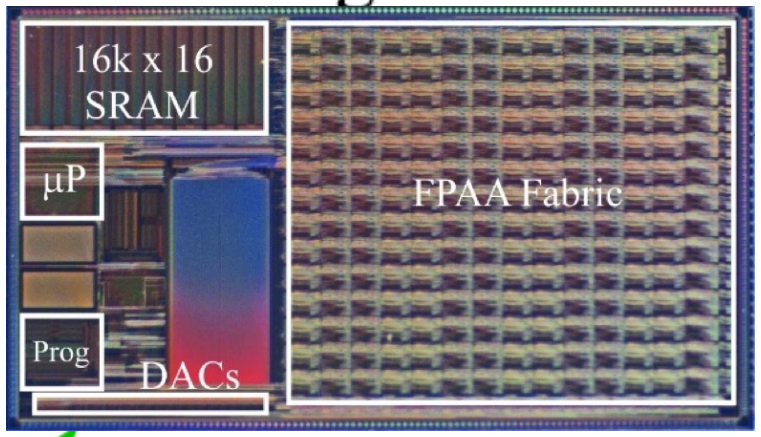
FPAA Tech File

GDSII (New IC)

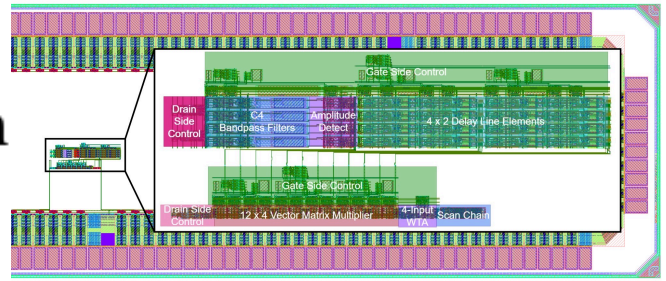
Targeted FPAA

[Ige, Yang, et. al 2023]
[Hasler & Cao, 2024]

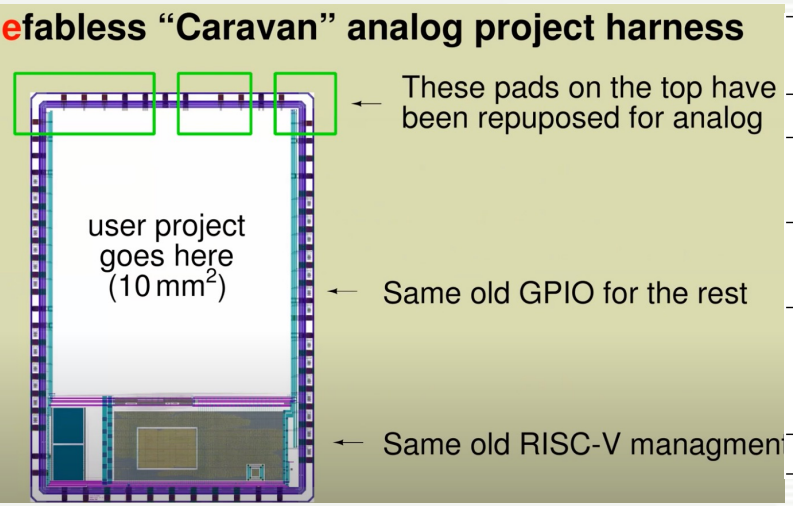
Existing FPAA



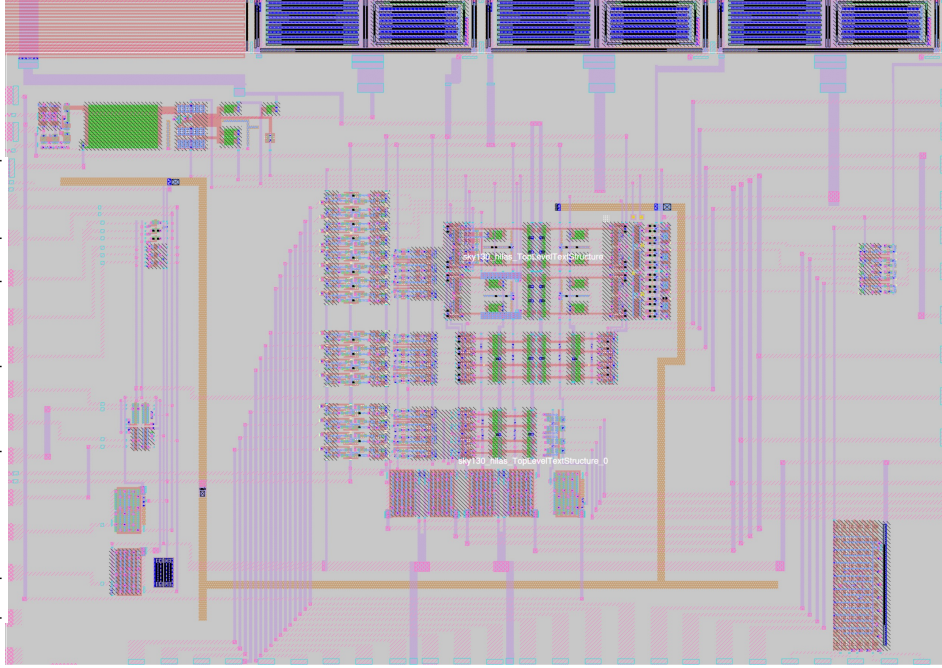
Custom device

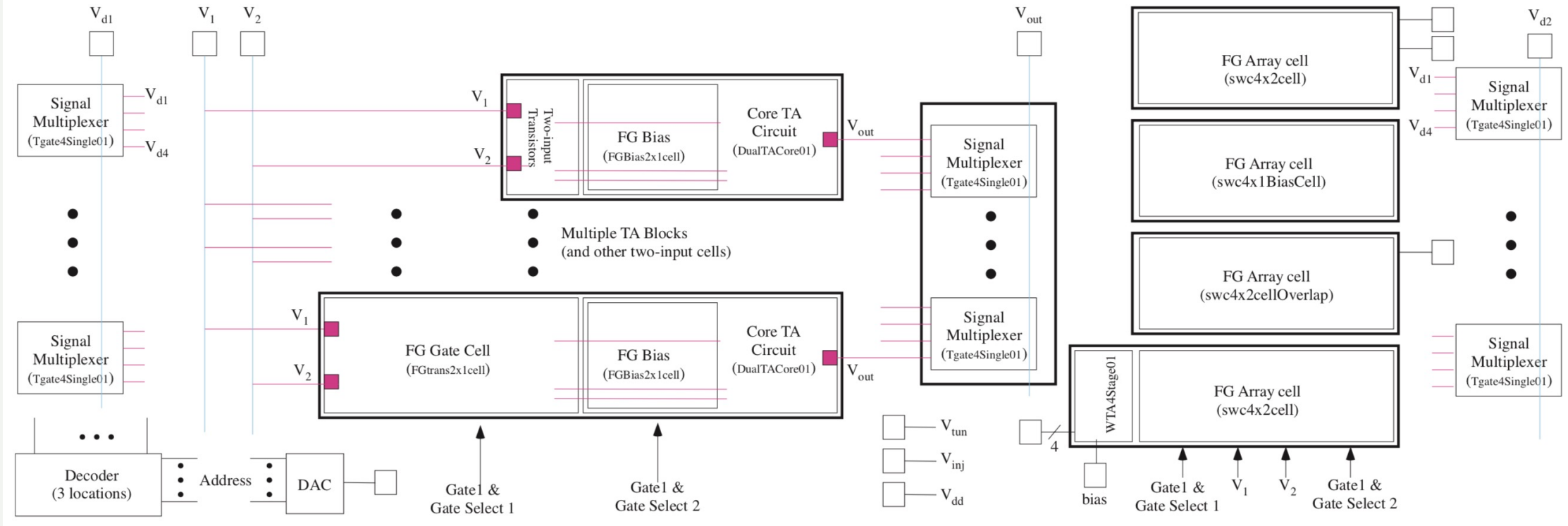


130NM STD CELL TEST STRUCTURE



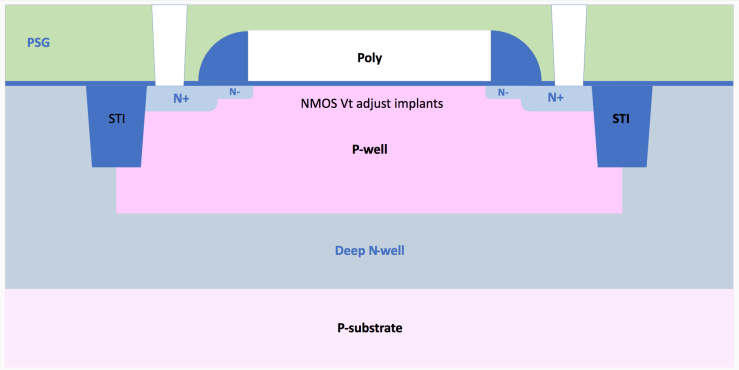
Block	pins	shared analog	shared digital
Supply	3 (GND, V_{dd}, V_{inj})	3	2
Transistors	8 (drains, shared sources)	V_g	
FG characterization	V_d (inj), V_{out} Cap In (2)	V_{tun} V_1, V_{ref}	
6 Sel Pins (64 cells)		V_{tun}	6
5 pin DAC	I_{out1}		
4 to 2 mux (TA out)	V_{TAout}		2
Total (29)	17	4	8

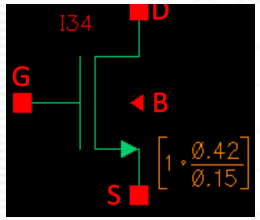


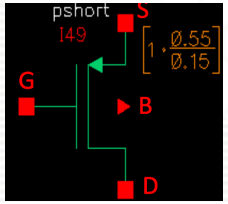


SKYWATER 130NM DEVICE DETAILS

1.8V NFET



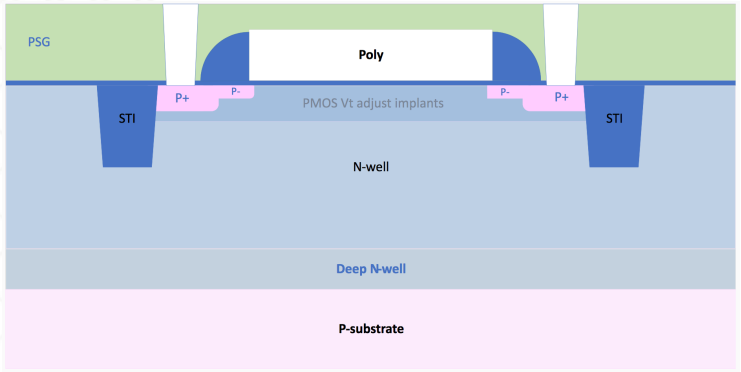




(sky130_fd_pr__nfet_01v8)

Thick Insulator for FG retention

1.8V PFET



(sky130_fd_pr__pfet_01v8)

Junction Diode Breakdown

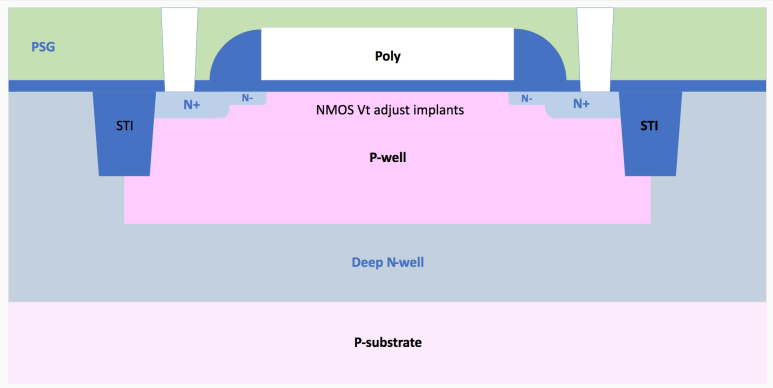
N+ breakdown ~ 10.7-11.5V
P+ breakdown ~ 10.2-12V
HV N+ breakdown ~12-12.5V
HV P+ breakdown ~11.2-12V

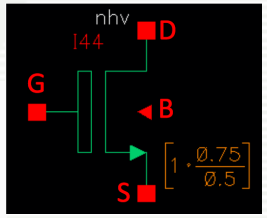
Conductor Sheet Resistances

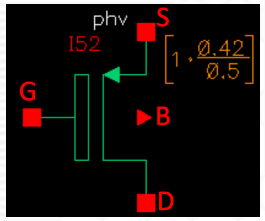
Nwell connection ~ 550-1350Ω/square
N+ connection ~ 100-133Ω/square
P+ connection ~ 166-233Ω/square
Poly gate~ 40-55Ω/square (typical)

Li connection ~ 10-15Ω/square
M1 connection ~ 0.1-0.15Ω/square
M2 connection ~ 0.1-0.15Ω/square
M3 connection ~ 0.04-0.05Ω/square
M4 connection ~ 0.04-0.05Ω/square
M5 connection ~ 0.02-0.035Ω/square

5/10.5V NFET

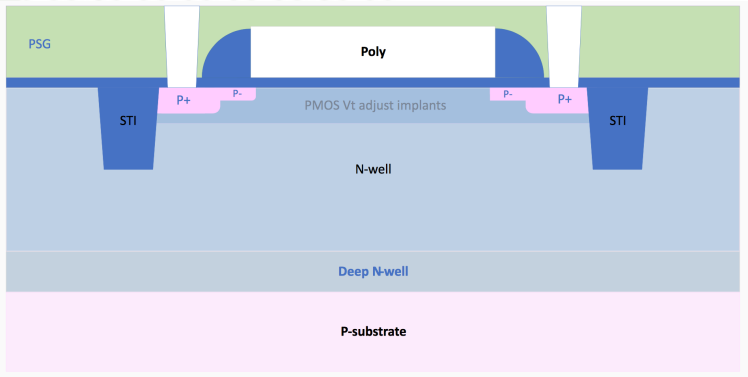






(sky130_fd_pr__nfet_g5v0d10v5)

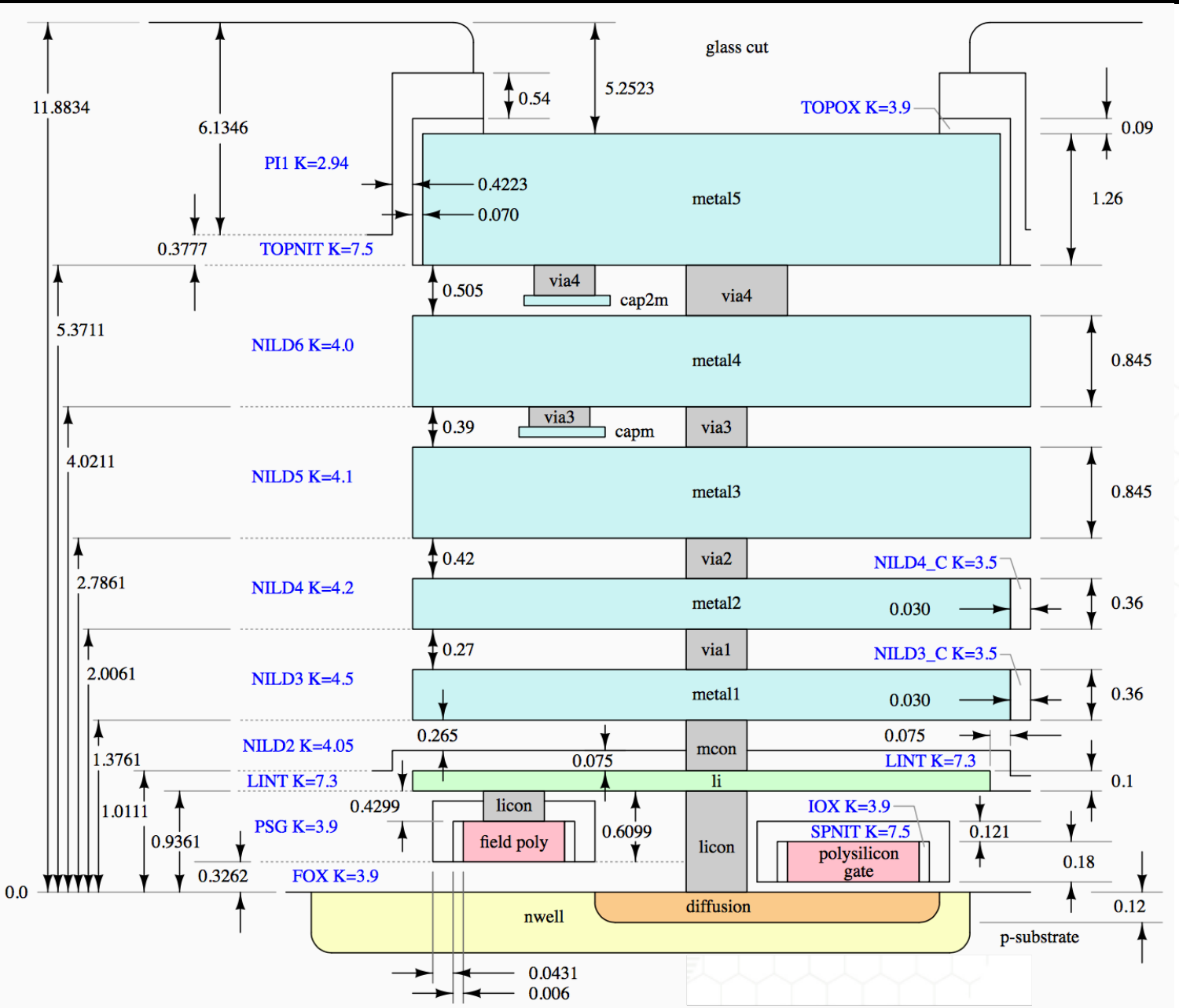
5/10.5V PFET

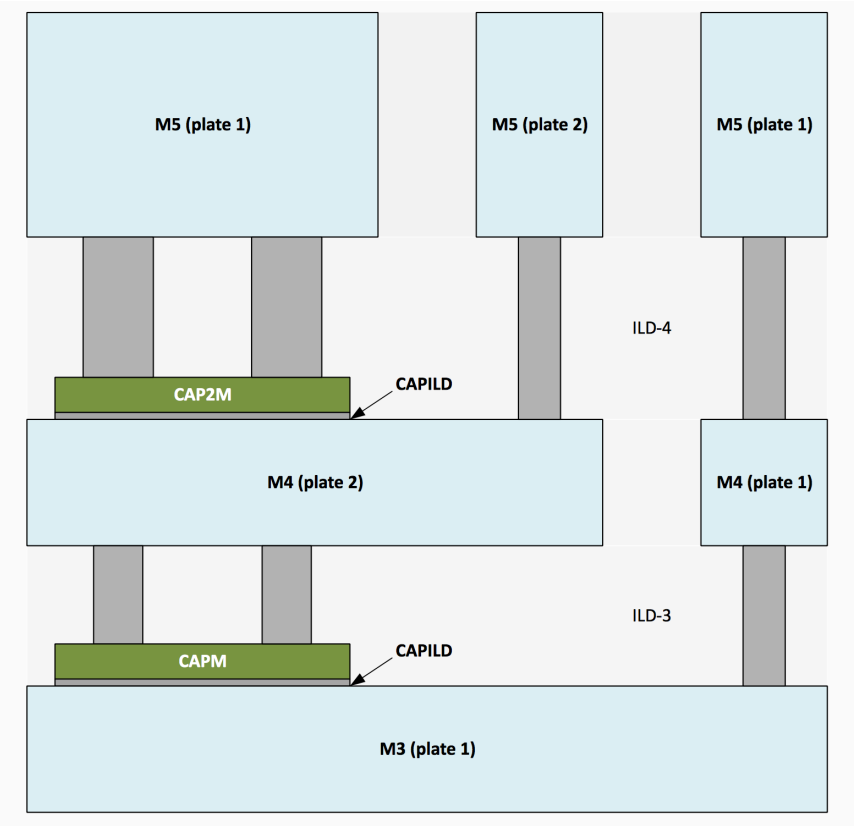


(sky130_fd_pr__pfet_g5v0d10v5)

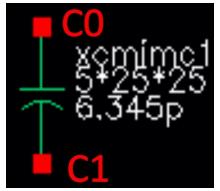
Device details: https://skywater-pdk.readthedocs.io/en/latest/rules/device-details.html

CORE SKYWATER LAYER MAP





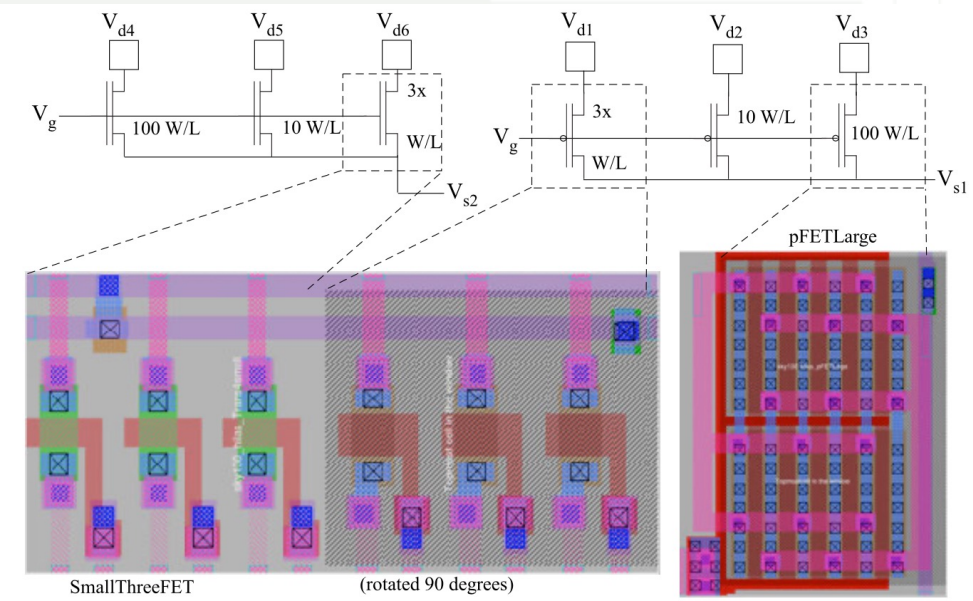
MIM capacitor (nwell)



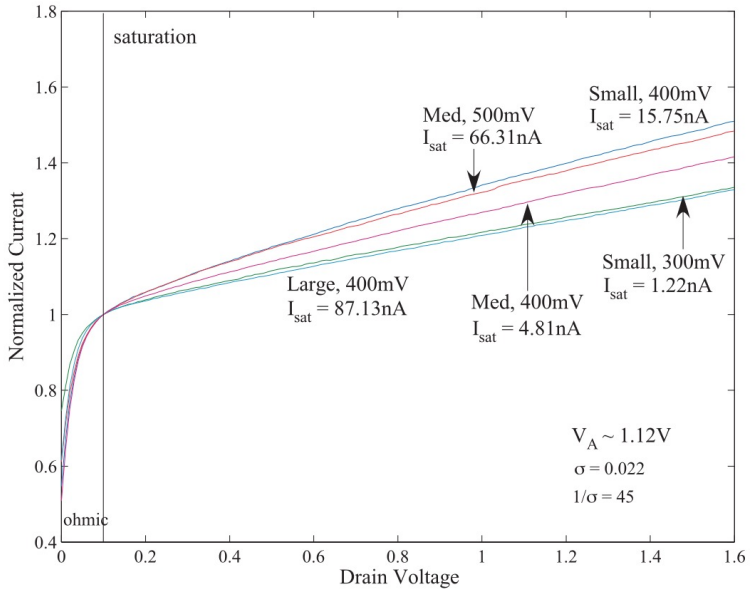
2.2fF/μm^2

(sky130_fd_pr__model_cap_mim)

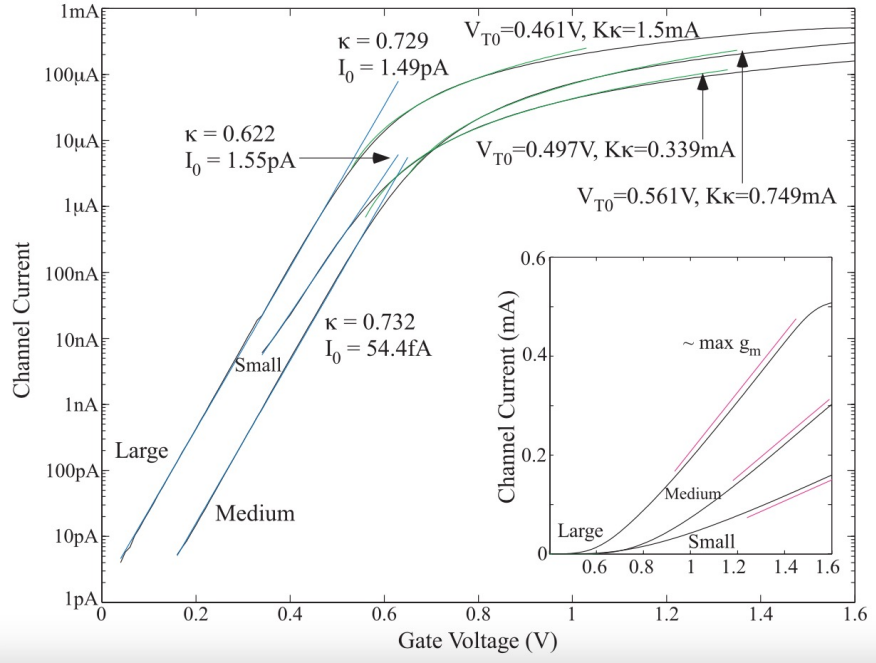
130NM TRANSISTOR CURVES & PARAMETERS

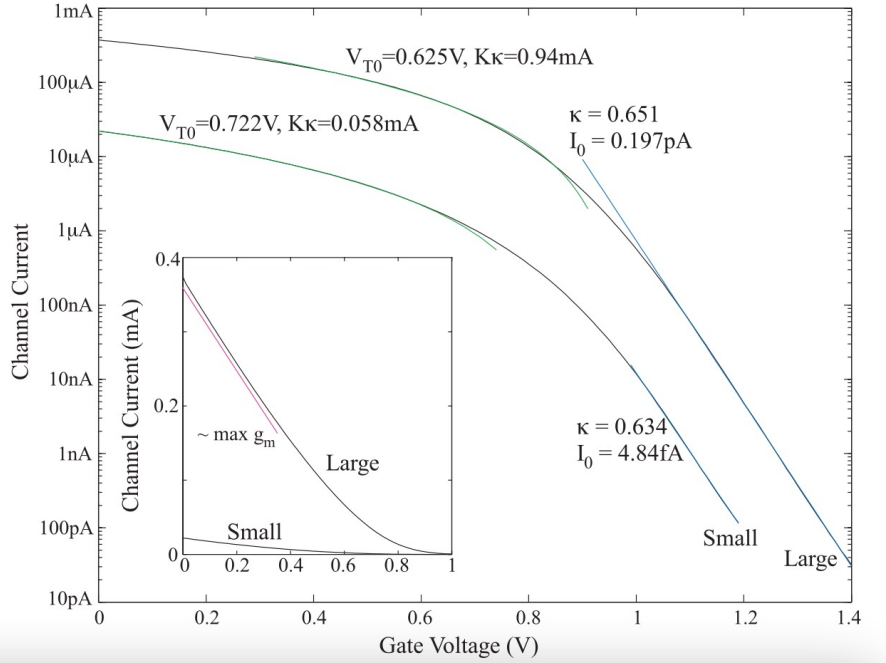


(a)

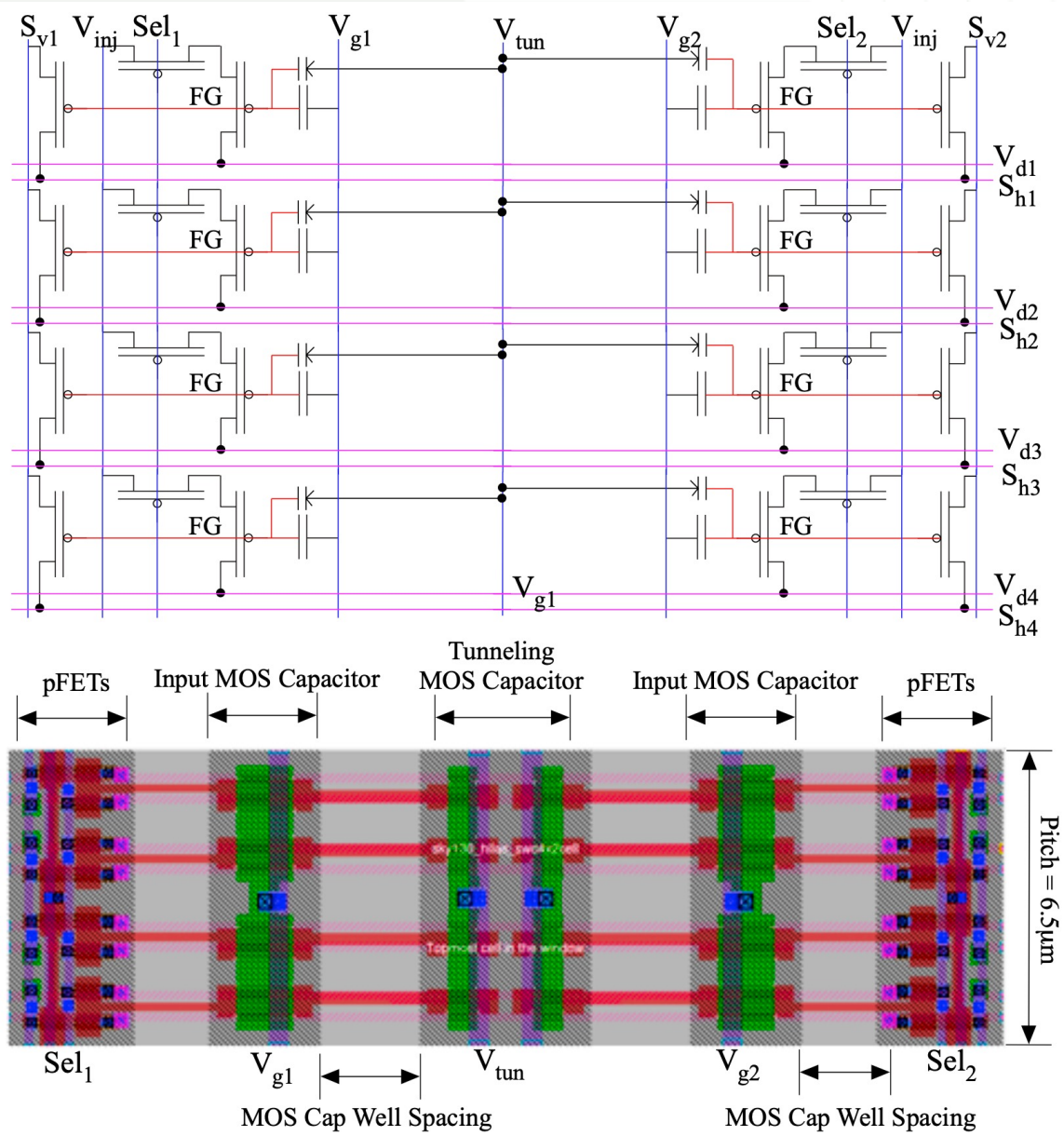


(b)

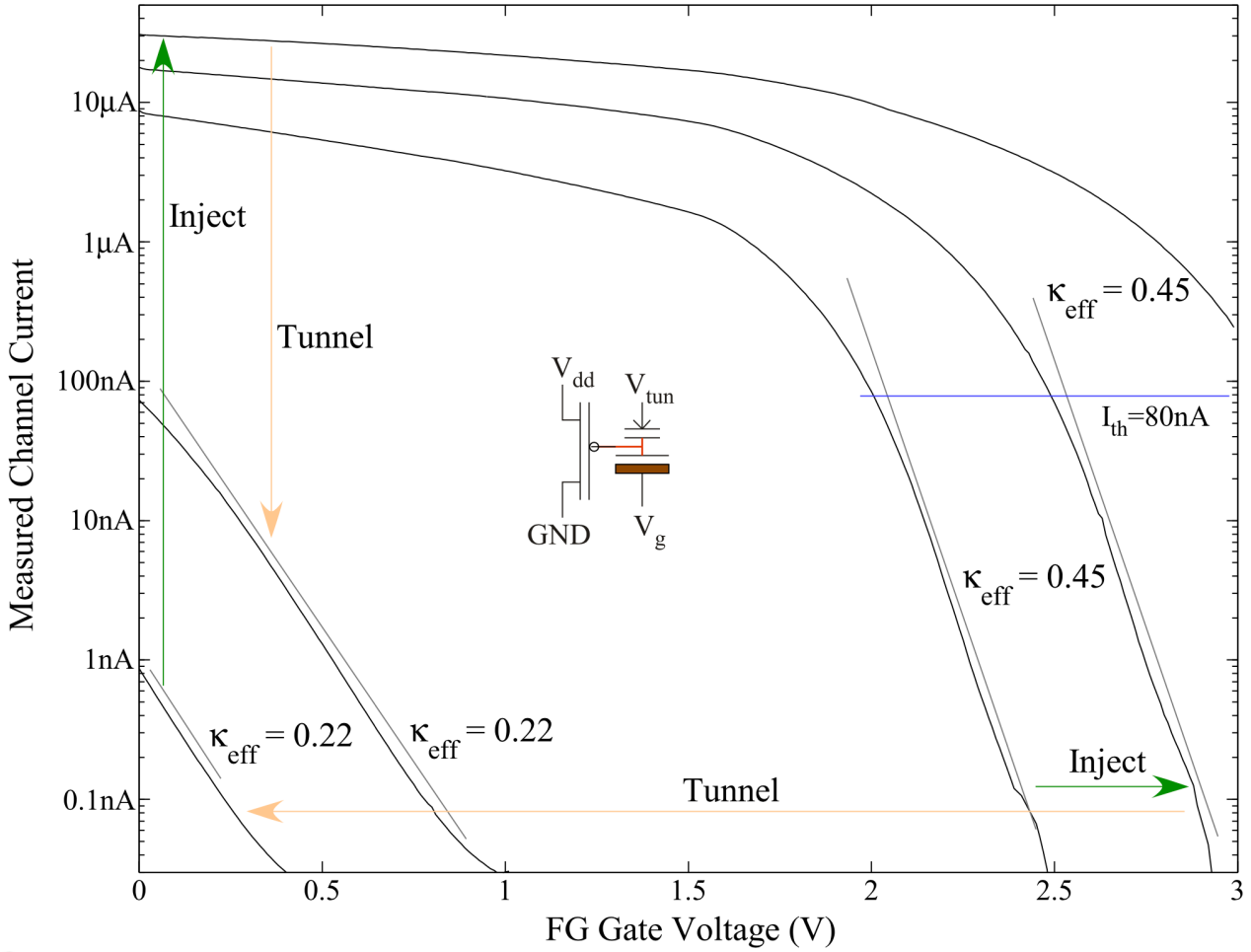




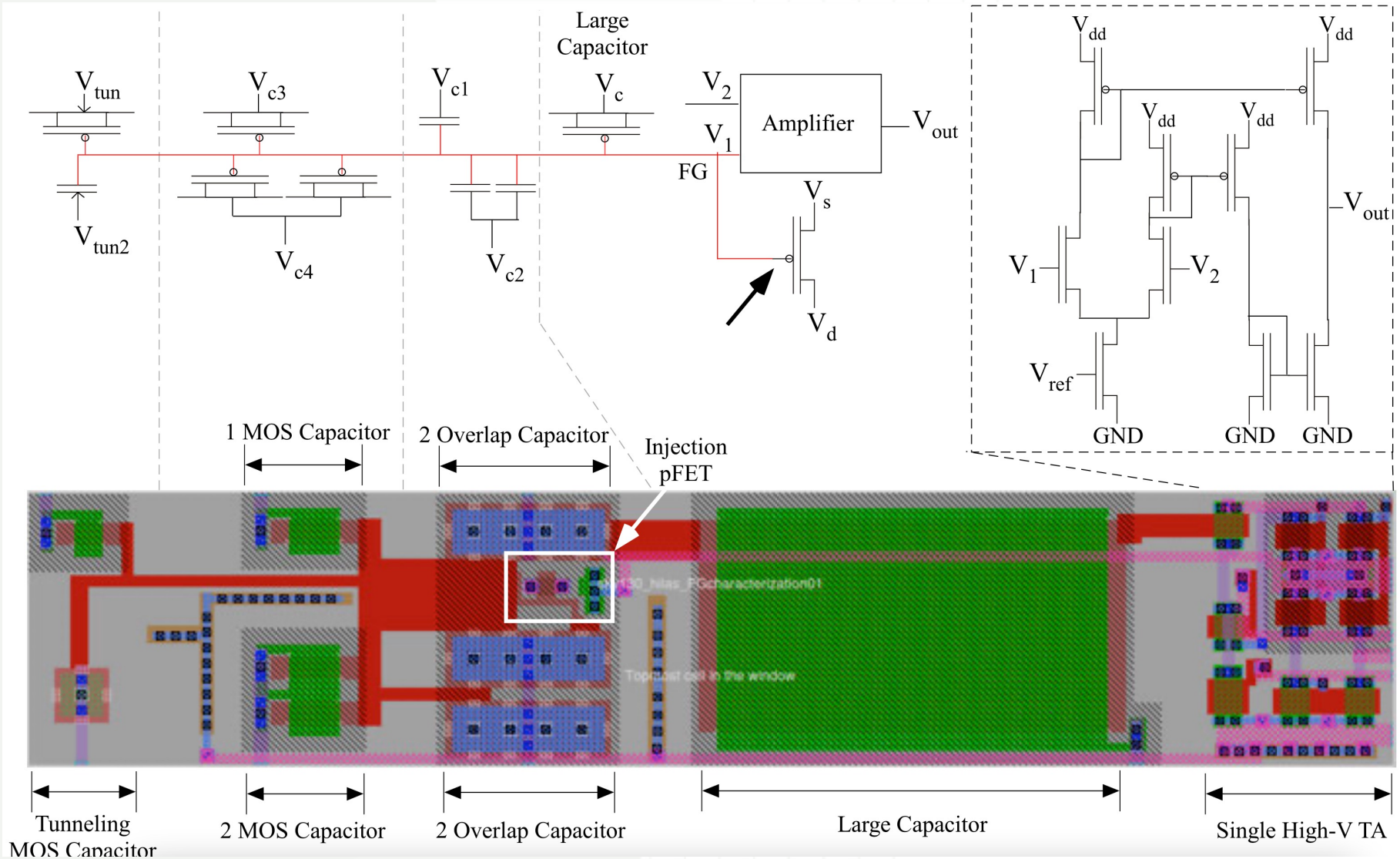
ANALOG STANDARD CELLS & FG PROGRAMMABILITY



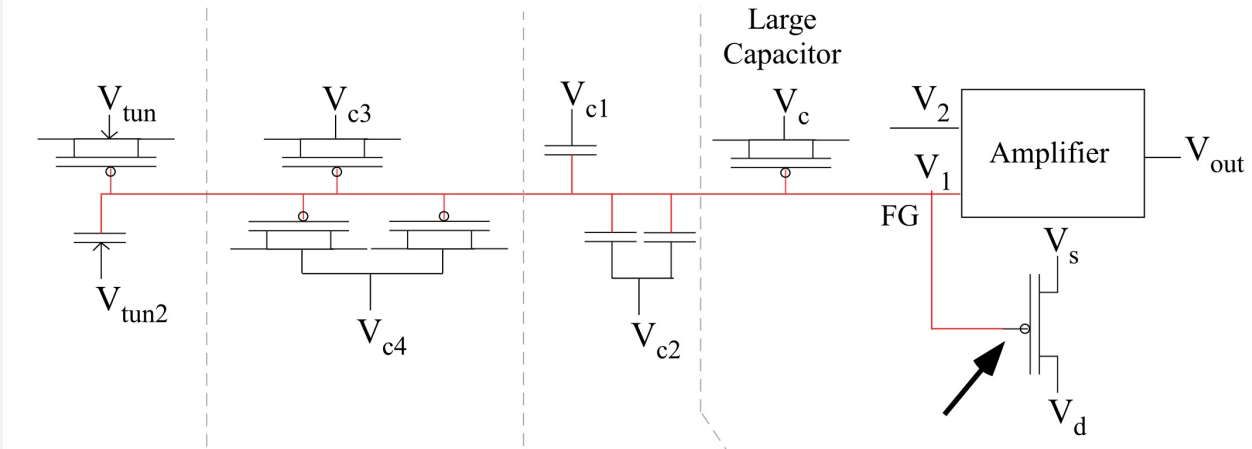
Tight FG arrays are essential everywhere
SWC 4x2 cell sets the pitch

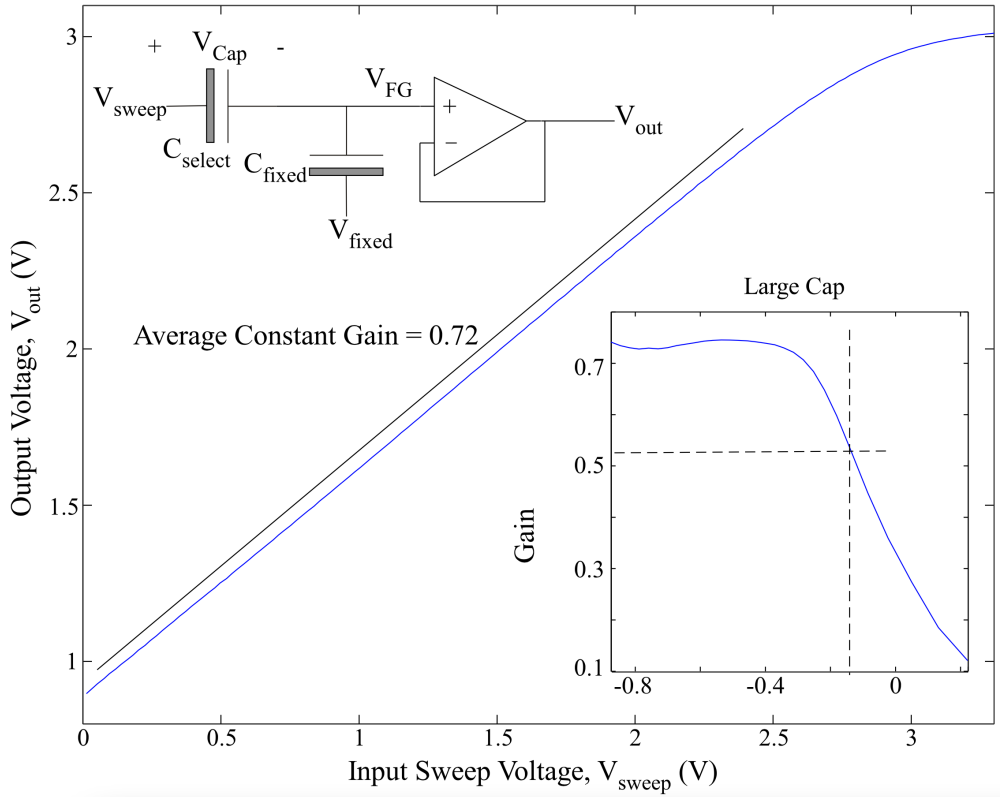


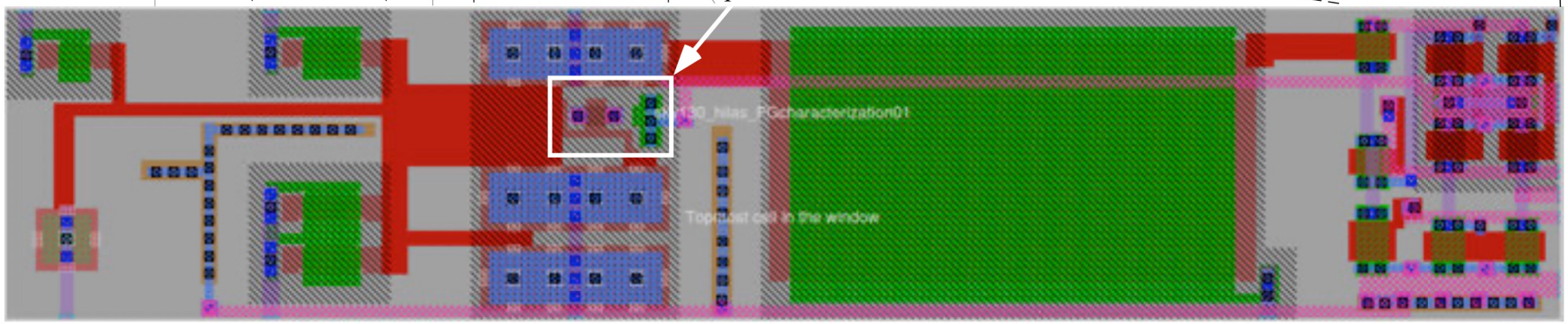
FG CHARACTERIZATION STRUCTURE



FG CHARACTERIZATION STRUCTURE

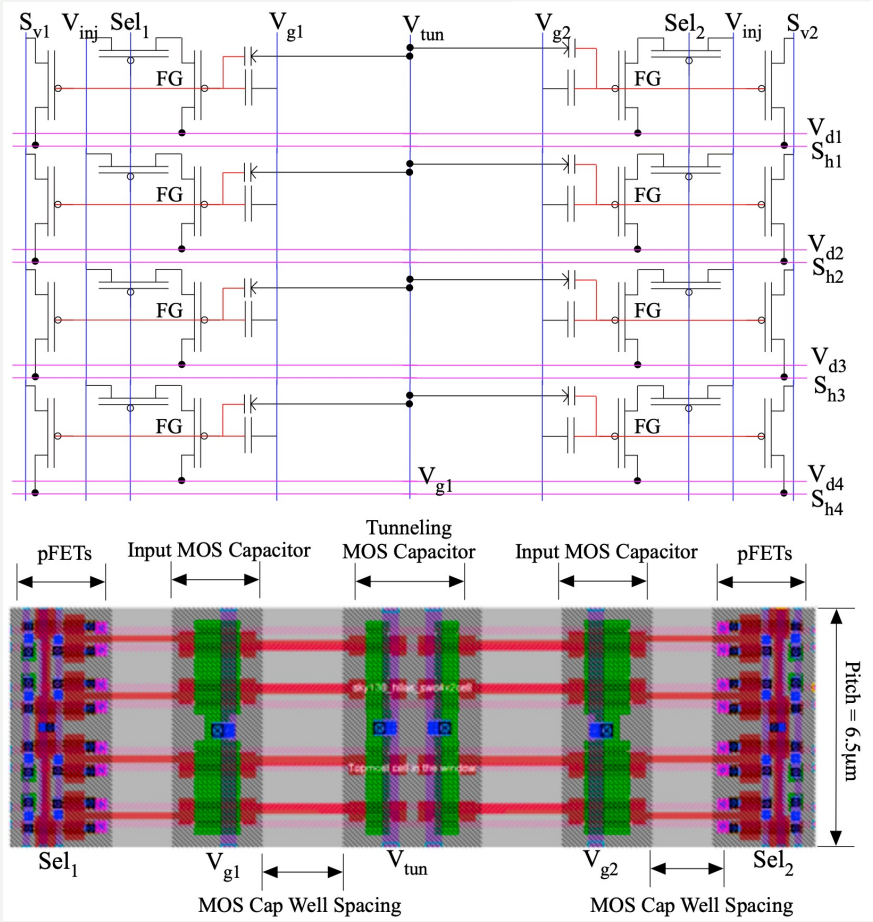






130NM STANDARD CELL LIBRARY

Std Cell libraries fabricated in 350nm, 180nm ,130nm, 65nm, 28nm, 16nm CMOS



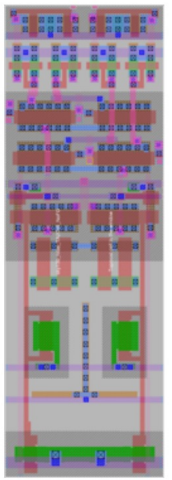
Analog Cells:

Cell Type	Variations	Name	Width
Transconductance Amplifiers (TA)	2 TA, FG bias, no FG inputs	TA2Cell_NoFG	17.92μm
	2 TA, FG bias, FG inputs (V_L large)	TA2Cell_1FG	28.09μm
	2 TA, FG bias, FG inputs (V_L small)	TA2Cell_1FG_Strong	28.10μm
	2 TA, signal bias, no FG inputs	TA2SignalBiasCell	8.45μm
Capacitors	Selectable 16 unit cap	capacitorArray01	36.70μm
	Two separate unit caps	capacitorSize04	5.78μm
	2 unit cap	capacitorSize03	5.79μm
	4 unit cap	capacitorSize01	10.42μm
	8 unit cap	capacitorSize02	7.97μm
Winner-Take-All (WTA)	4 WTA stages	WTA4Stage01	14.07μm
Ratioed Transistor DAC Modules	5 bit transistor module	DAC5bit01	16.58μm
Transmission Gates	4 Single Throw T-gates	Tgate4Single01	4.76μm
	4 Double Throw T-gates	Tgate4Double01	7.08μm
	4 T-gate for prog select (V_{inj})	drainSelect01	5.42μm
Transistors (nFET + pFET)	3 nFETs + 3 pFETs (W/L≈1)	Trans4small	2.80 μm
	2 nFETs + 2 pFETs (W/L≈10)	Trans2med	3.53μm
	1 nFETs (W/L≈100)	nFETLarge	4.37μm
	1 pFETs (W/L≈100)	pFETLarge	4.64μm

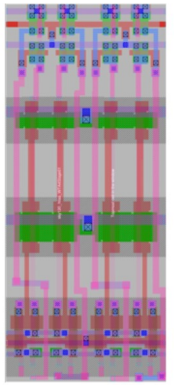
FG Cells:

Cell Type	Variations	Name	Width
Crossbar Cell (Same C_T)	4×2 Cell	swc4x2cell	20.12μm
	4×1 Bias	swc4x1BiasCell	10.11μm
	4×1 cell	swc4x1cell	10.08μm
FG Gate cell (Same C_T)	2 x 1 FG Biases	FGBias2x1cell	11.53μm
	2 x1 FG Transistors	FGtrans2x1cell	11.52μm
	2 x1 FG Trans, small input C	FGBiasWeakGate2x2cell	11.53μm
FG Characterization cell	Tun, pFET (inj), Capacitors	FGcharacterization01	29.95μm

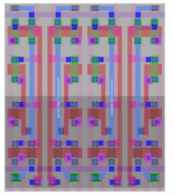
TA2Cell noFG



WTA4Stage01

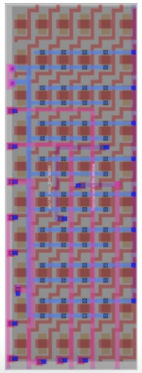


Tgate4Double01

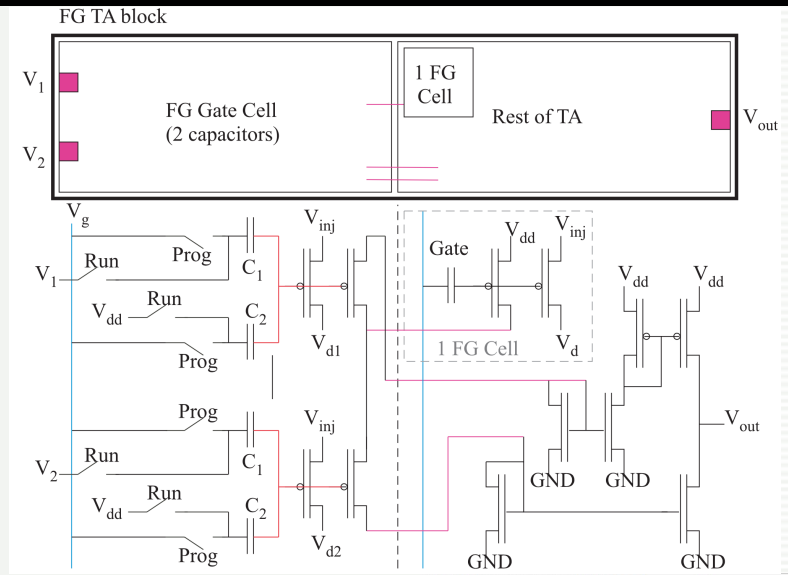


capacitorArray01

DAC5bit01

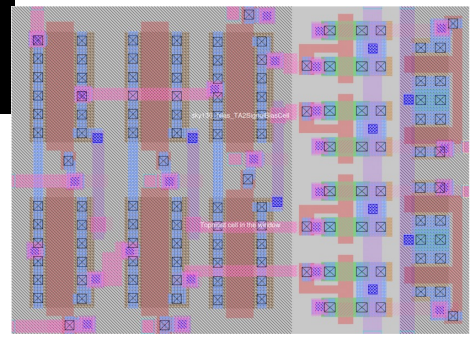


TRANSCONDUCTANCE AMPLIFIERS (TA)

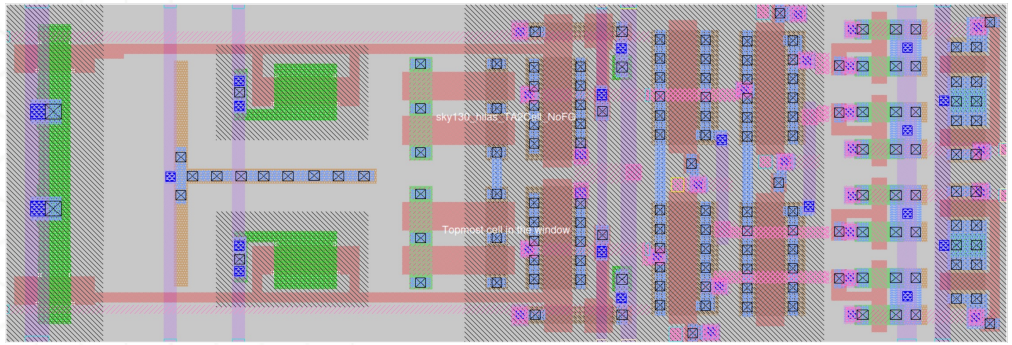


Pitch and Width Matched to swc4x2cell

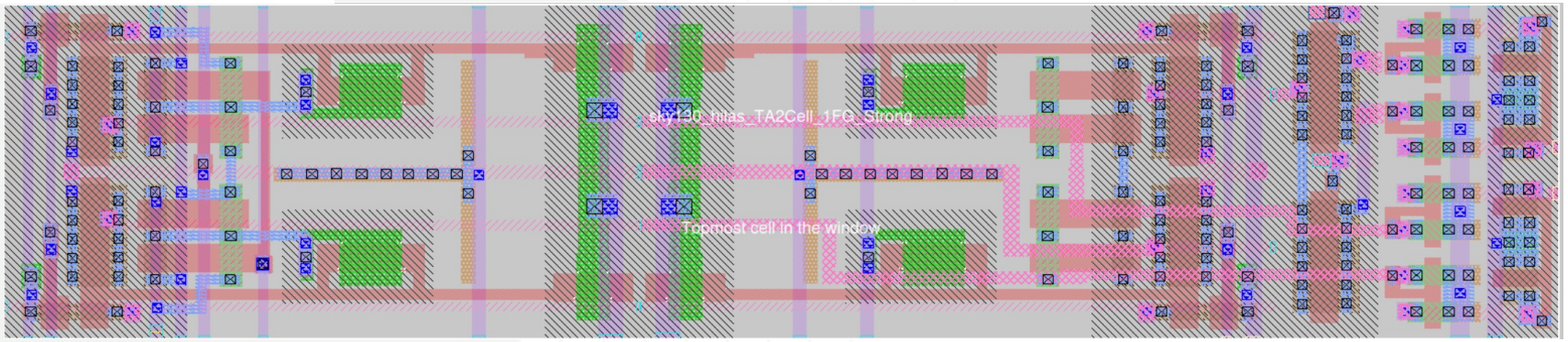
TA2SignalBiasCell



TA2Cell_NoFG



TA2Cell_1FG_Strong



TA2Cell_1FG