Layout Aware LUT Design Exploration

Daniel Arévalos Ortiz

AEMY Team - Hochschule München University of Applied Sciences

Why Layout-Aware Exploration?

Electrical LUT-based exploration enables the efficient evaluation of large analog design spaces[1]. However, pre-layout electrical LUTs do not capture local interconnect parasitics or the geometry-dependent capacitance of physical implementations.

Complete layout generation and parasitic extraction can recover these effects, but performing full PEX for every candidate is computationally expensive.

Proposed Approach

Electrical device behavior and local physical effects are characterized offline and stored in independent LUTs. During design-space exploration, both models are queried and combined within the same MNA circuit representation.

1. Generate a pre-layout electrical MOS LUT.
2. Extract reusable PEX-derived multiport models from parameterized physical primitives.
3. Map and stamp the electrical and physical matrices into the circuit MNA system.
4. Validate selected candidates against complete circuit-level layout and PEX simulation.

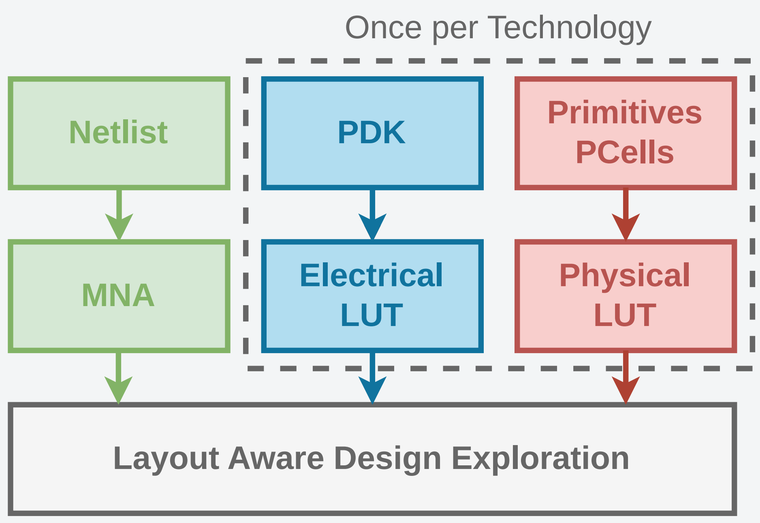

Figure: General Approach.

Pre-Layout Electrical LUT Generation

Technology-specific compact models are characterized offline using NGSpice. A MOS transistor finger is evaluated over the five-dimensional design and operating-point space

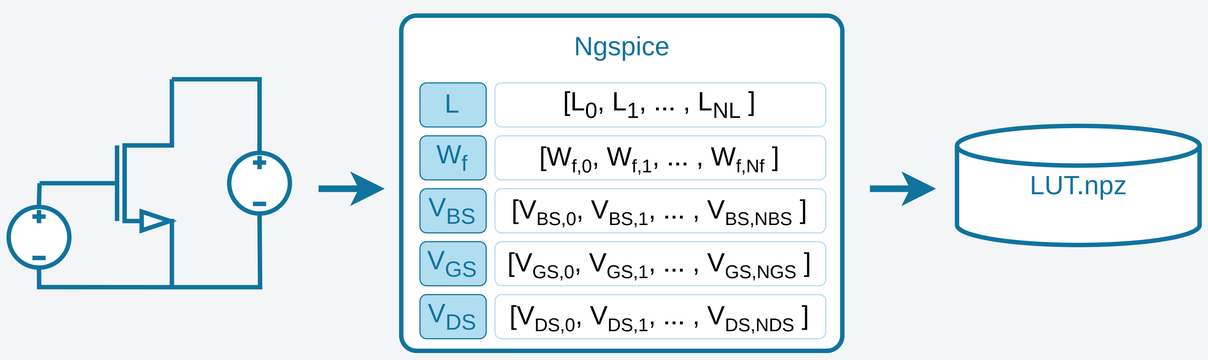

Figure: Electrical LUT Generation.

$$\boldsymbol{q}_{\mathrm{elec}} = (L,\ V_{\mathrm{BS}},\ V_{\mathrm{GS}},\ V_{\mathrm{DS}},\ W_f)\,,$$

where W_f is the width of one transistor finger.

The resulting LUT stores drain current, small-signal conductances, intrinsic charge derivatives, and compact-model overlap and junction capacitances:

$$\mathcal{L}_{\mathrm{elec}}\left(\boldsymbol{q}_{\mathrm{elec}}\right) \rightarrow \left\{I_D,\ g_m,\ g_{ds},\ \mathbf{C}_{\mathrm{MOS}}\right\}.$$

Nine independent intrinsic charge derivatives are stored. Charge conservation is then used to reconstruct the complete 4×4 terminal capacitance matrix before it is converted into nodal form for MNA stamping.

During exploration, interpolation and inverse-current sizing determine the per-finger width W_f, an integer finger count n_f, and the complete electrical small-signal model of each candidate.

$$(L,\ V_{\mathrm{BS}},\ V_{\mathrm{GS}},\ V_{\mathrm{DS}},\ I_{D,\mathrm{target}}) \longrightarrow (W_f,\ n_f,\ g_m,\ g_{ds},\ \mathbf{C}_{\mathrm{MOnnS}})$$

References

[1] Arévalos, D., Marin, J., Herman, K., Gomez, J., Wallentowitz, S., Rojas, C. A. (2025). *ATopology-Independent and Scalable Methodology for Automated LDO Design Using Open PDKs.* Electronics, 14(17), 3448. https://doi.org/10.3390/electronics14173448

Contact

Daniel Arévalos Ortiz
Hochschule München, AEMY Team
daniel.arevalos@hm.edu

PCell-Based Physical LUT Generation

The physical LUT is generated offline for reusable layout primitives. A deterministic PCell maps each transistor geometry to a complete primitive layout with a fixed set of logical ports.

$$\boldsymbol{q}_{\mathrm{geom}} = (L, W_f, n_f)$$

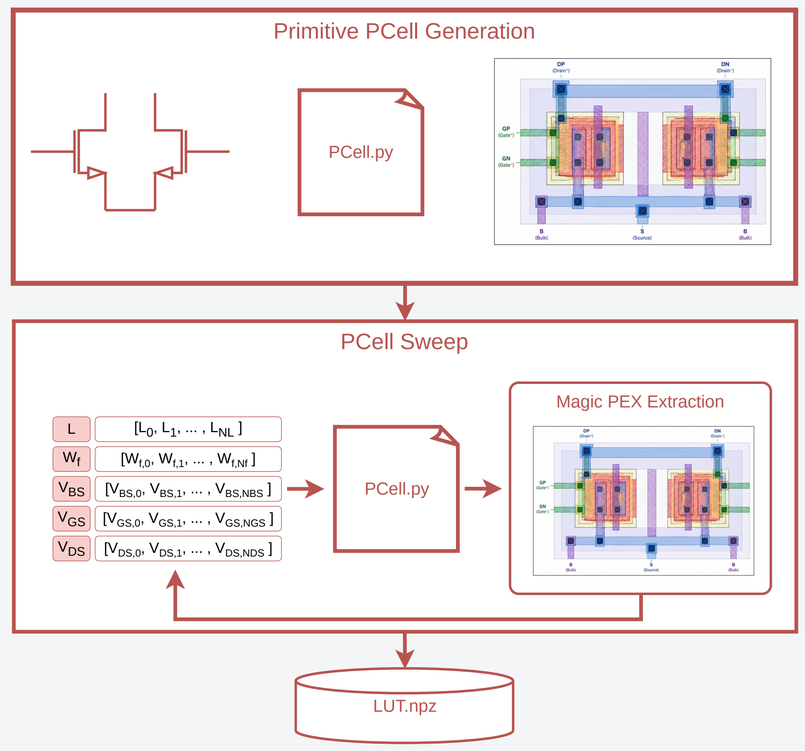

Figure: Layout aware LUT Generation.

1. Local interconnect extraction

For every geometry point, the PCell is exported to GDS and extracted with Magic:

$$\mathbf{G}_{\mathrm{int}}\left(\boldsymbol{q}_{\mathrm{geom}}\right), \qquad \mathbf{C}_{\mathrm{int}}\left(\boldsymbol{q}_{\mathrm{geom}}\right).$$

2. Post-layout device correction

The capacitance of the multifinger devices inside the PCell may differ from that of an aggregate compact model:

$$\Delta\mathbf{C}_{\mathrm{dev}} = \mathbf{C}_{\mathrm{PEX,MOS-only}} - \mathbf{C}_{\mathrm{aggregate}}.$$

The physical LUT therefore provides

$$\mathbf{C}_{\mathrm{phys}} = \mathbf{C}_{\mathrm{int}} + \Delta\mathbf{C}_{\mathrm{dev}}.$$

Layout-Aware Matrix Composition

Electrical and physical LUTs are queried using the geometry and operating point of each circuit candidate. The electrical LUT provides the compact device model, while the physical LUT provides local primitive-level corrections:

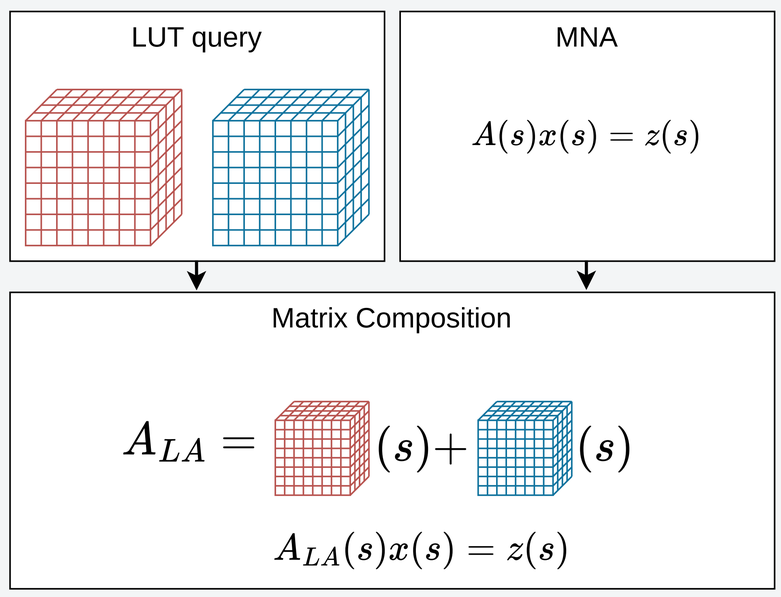

Figure: Matrix Composition.

The physical LUT complements the compact electrical model; it does not replace its intrinsic and extrinsic device capacitances.

Results

A four-transistor OTA is used as a compact validation example. Its differential pair and current mirror are modeled as independently characterized physical primitives, enabling comparison between the layout-aware prediction and complete circuit-level PEX simulation.

Table: Comparison table.

Flow	Time/Candidate	Speedup	Gain Error	$f_{3\mathrm{dB}}$ Error	UGF Error	PM Difference
Electrical + Physical LUT	$\approx 0.28\,\mathrm{ms}$	$\approx 1491\times$	0.024%	2.19%	14.50%	3.58°
Electrical + Magic PEX + NGSpice	$\approx 421\,\mathrm{ms}$	$1\times$	Reference	Reference	Reference	Reference