Towards a general-purpose RISC-V core for amateur radio transmission schemes

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Motivation

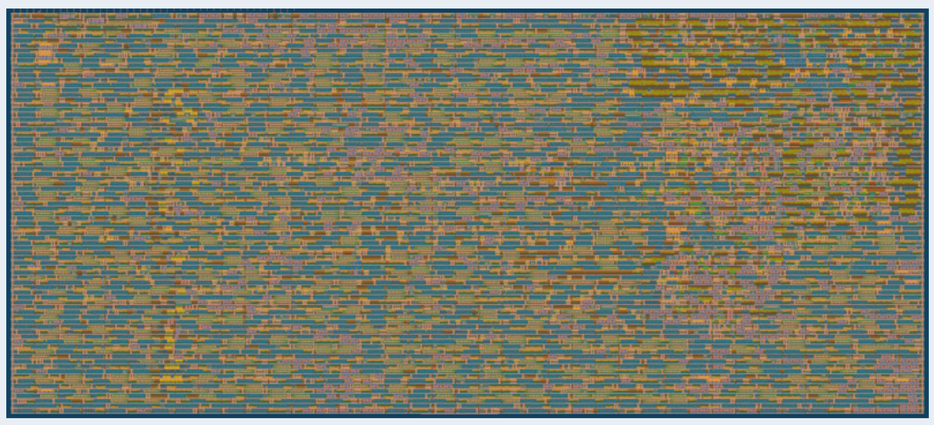
- Learn CPU design
  - Multi-Cycle design without pipelining
  - UART and I2C communication with peripherals
  - Interrupts and timers
- Learn to design chips with FOSS tools
- Create a bachelor's course where students build a CPU and learn about assembler programming
- Build a general-purpose digital core for WSPR

Current applications

- Use in lectures
- Digital building block for TinyWhisper
  - WSPR: digital transmission scheme in amateur radio
  - CPU is extended with a 30-bit CORDIC and Delta-Sigma modulators to generate sine waves
  - C program reads callsign, locator and power from the user and generates the signal
  - Analog filtering is done externally or with an analog front-end on the chip

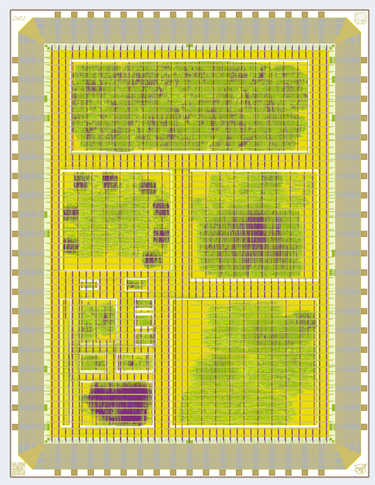
2024: Skywater 130nm (Tiny Tapeout 6)

- First tapeout of the CPU
- ISA initially only based on TinyRV1
- Very few instructions
- External SPI memory required
- On-board the HUNITY satellite
- SPI memory emulated with the RP2040 in software
- Successfully tested in space



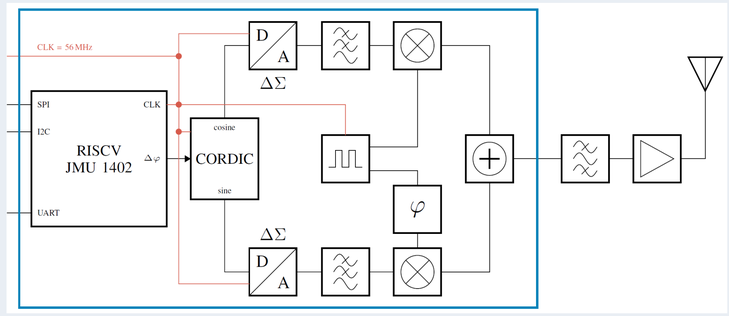
2025: Globalfoundries 180nm (wafer.space)

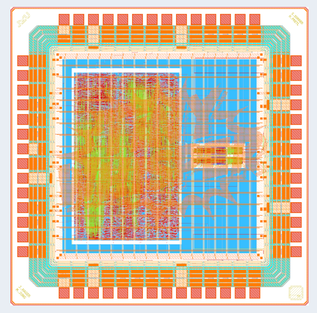
- Made possible by JKU Linz
- rv32e_zicsr ISA
- Running at 28 MHz
- Digital design of TinyWhisper only, the PWM outputs have to be filtered externally
- In addition to the CPU: different projects from JKU and HTL students
- Chip has been assembled and first tests show promising results



2026: IHP 130nm

- Digital core and analog front-end on the same tapeout
- Analog front-end by Simon Dorrer (JKU Linz)
- Design running at 56 MHz
- Still in production, expected in December 2026





Next steps

- Design a PCB with SRAM, RF amplifiers, bandpass filters
- Create a 3D-printed enclosure with buttons, display and batteries
- Implement other transmission schemes (FT8, CW)
- Attach an antenna and test the chip outside of a controlled lab environment

Further information