Open-Source Chip Design in Education with Tiny Tapeout

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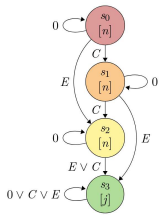
Motivation

- FPGAs are a popular development platform
- Open-Source FPGA tooling is getting more mature
- ASICs offer more performance and versatility
- Workflow can be similar, but producing ASICs is very expensive
- Hard to learn about chip design or produce chips for research and teaching

Educational purposes

- Accessible to Students
  - Cost-Effective, Community-Driven Chip Production
  - Open-Source Toolchain (Yosys, OpenROAD, Magic, ...)
  - Open-Source PDKs (SkyWater 130 nm, IHP 130 nm, ...)
- Lecture Examples and Hands-On Demonstrations
  - Finite State Machine (FSM) Implementation
  - Physical Demonstration of Adder Architectures

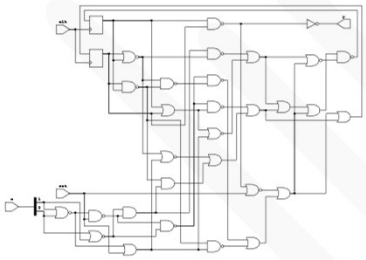
The design flow:




```
always_comb begin
    state_d = state_q;
    if(x == 2'b01) begin
        case(state_q)
            z0   : state_d = z50;
            z50  : state_d = z100;
            z100 : state_d = z150;
            z150 : state_d = state_q;
        endcase
    end else if(x == 2'b10) begin
        case(state_q)
            z0   : state_d = z100;
            z50  : state_d = z150;
            z100 : state_d = z150;
            z150 : state_d = state_q;
        endcase
    end
```

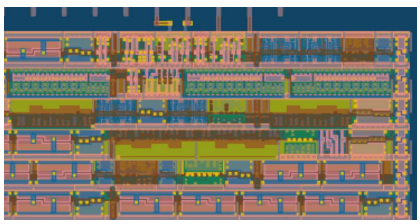
Synthesis with Yosys

- Converting VHDL/SystemVerilog to Verilog
- Analysing Verilog module
- Producing and optimizing netlist



ASIC flow with OpenLane

- Floorplanning
- Placement
- Static Timing Analysis
- Clock Tree Synthesis
- Global Routing

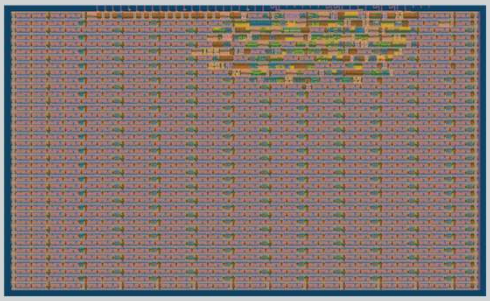


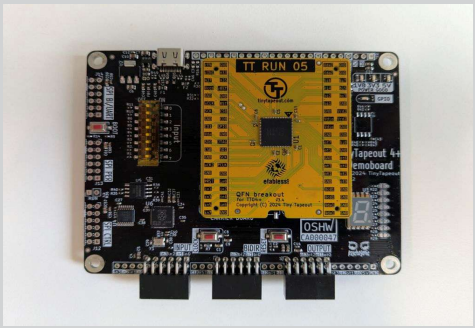
TTo5

- Submitted: 04.11.2023
- Size: 157 Standard cells
- Written in: VHDL

Description:

- First test run
- 4-Bit ALU containing:
  - Ripple-Carry adder
  - Carry-Lookahead adder
  - Matrix Multiplier
  - Wallace Tree
  - Barrel-Shifter
  - Comparator
- Chip can be controlled with the on-board RP2040 and a Python shell
- Unclocked IOs allow measurements of the critical path of the ALU modules



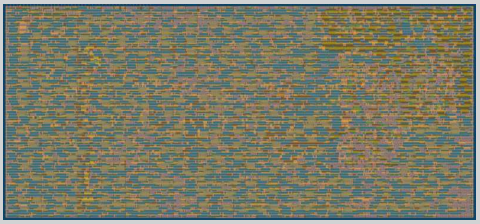


TTo6

- Submitted: 19.04.2024
- Size: 6655 Standard cells
- Written in: VHDL/SystemC

Description:

- TinyRV 1 compliant RISC-V CPU
- SPI Interface to external memory
- 12 MHz target clock rate
- Today in Space



TTo8

- Submitted: 06.09.2024
- Size: 1062 Standard cells
- Written in: SystemVerilog

Description:

- State machine from lectures
- 8-Bit to 24-Bit serial decoder
- 24-Bit Ripple-Carry adder
- 24-Bit Carry-Lookahead adder
- Different critical paths can be measured
- Additional tapeout with IHP Open-Source PDK