Memory Controller for LPDDR4

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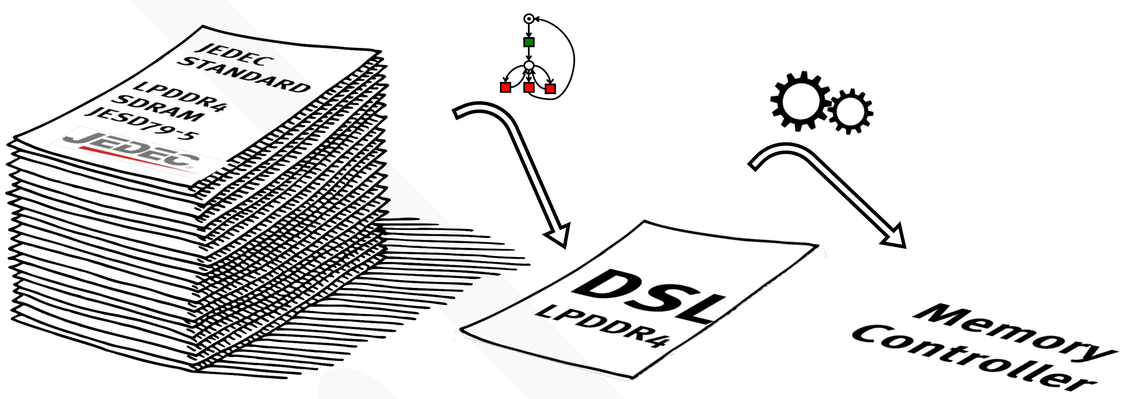
Computer Engineering 17

Motivation

- Creating a memory controller out of a new JEDEC specification can be complicated
- AI cannot create a memory controller out of the specification (yet)
- A Domain Specific Language (DSL) can simplify this process

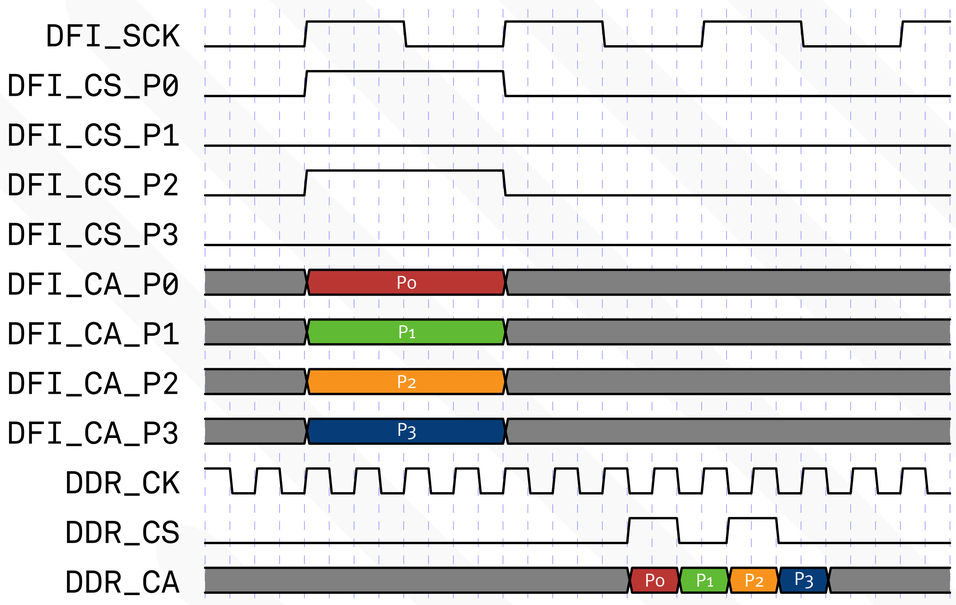


Contents of a JEDEC Standard

- Physical description
- Command encoding
- State diagram of a bank
- Timing diagrams of each command
- Initialization and training

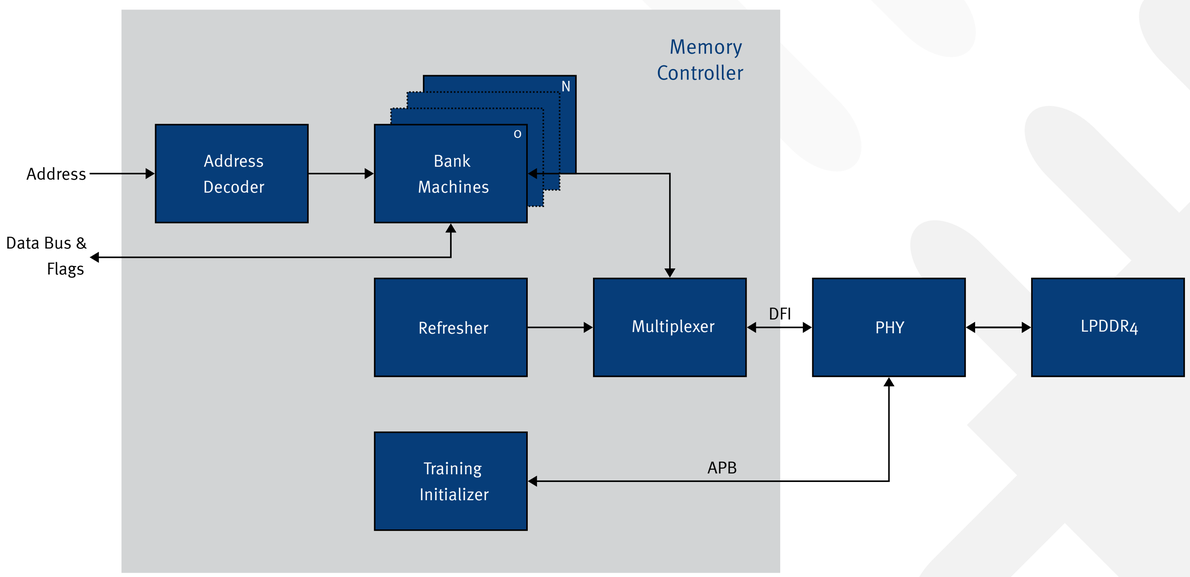
PHY

- PHY and memory controller connected by DFI
- The PHY gets trained to the physical characteristics of the memory
- Because of the high speed of the memory, the controller runs slower. This is called Gearing factor, e.g. 4:1.
- The PHY has to serialize the requests of the memory controller

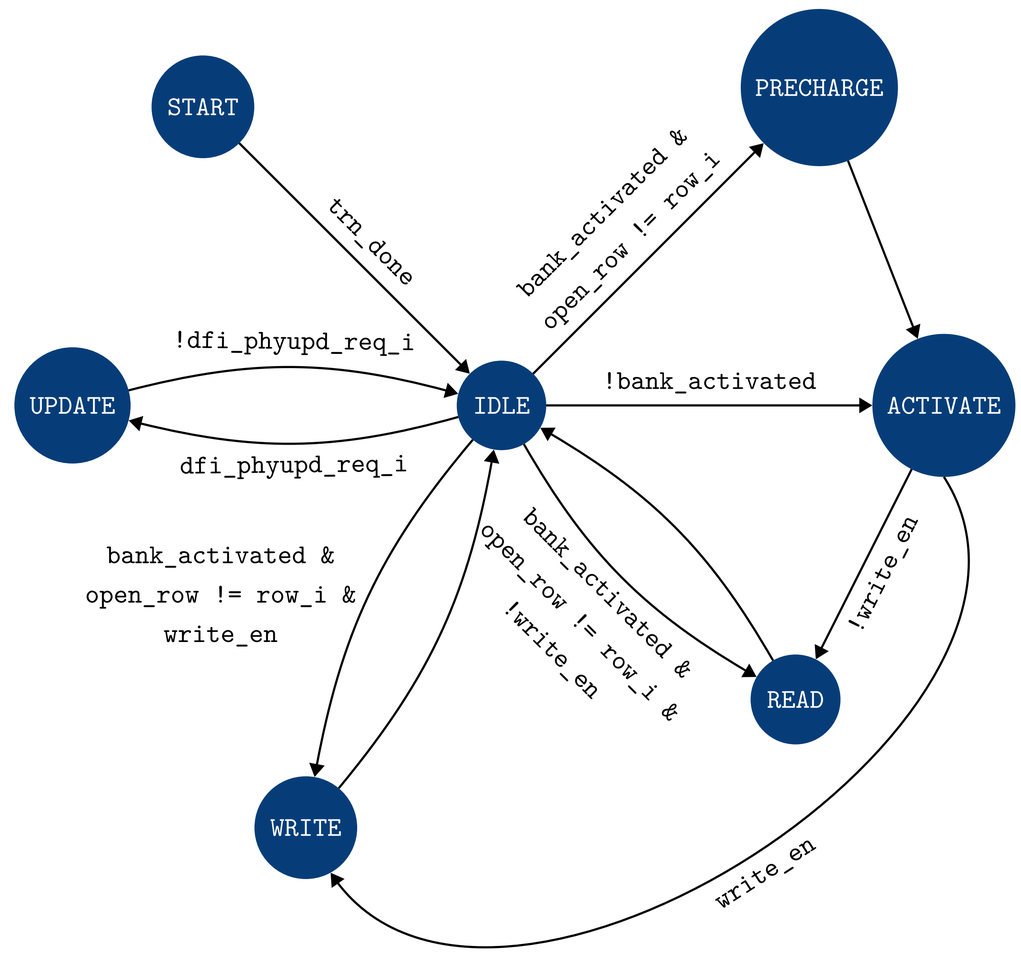


Memory Controller

- The address gets decoded into bank, row and columns
- There is one **Bank Machine** for each bank which generates the commands
- The **Refresh Machine** sends a refresh command after a period
- The multiplexer selects which machine is allowed to send the command



State Diagram of a Bank Machine



Code Generation

The code generation is done in Python using the Jinja templating engine. The engine allows using loops and to set values using the DSL file.

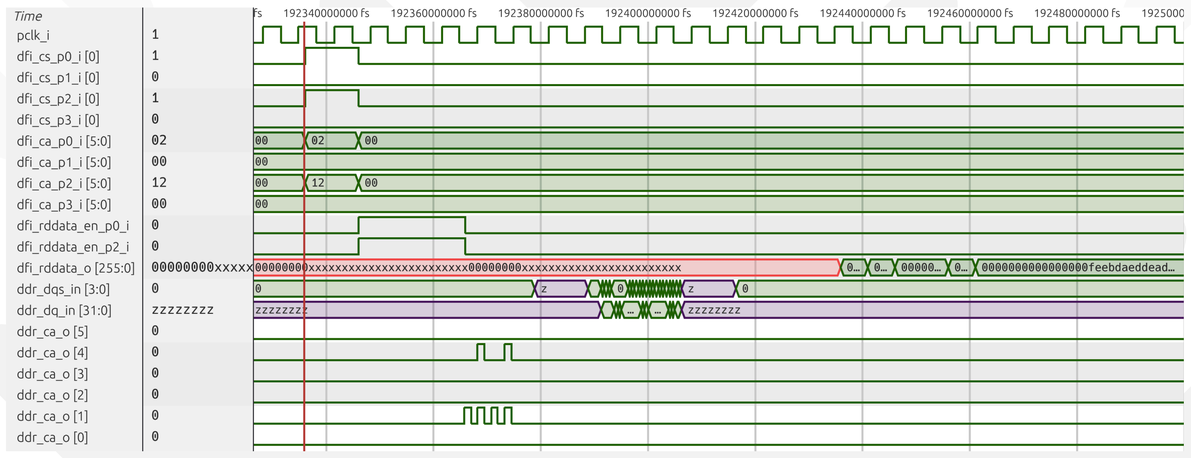
Python Code Example

Jinja

```
{% for bank in range(number_of_banks) %}
  // Bank Machine {{bank}}
  // States
  states_memcon state_m{{bank}}, next_state_m{{bank}};
  {# Here is the rest of the code #}
{% endfor %}
```

Results

The following figure shows one read request. The top part is the DFI interface and below there is the memory interface. You can see the delay between sending the command from the controller to the memory.



Future Work

- Instruction queue with scheduler
- Test it on the Lattice Avant Evaluation Board
- Combining the two parameter files
- Improving the generator
- Power features
- AXI Interface
- Mask writes
- Testing different features on the memory controller