The FABulous Open FPGA Framework

Novel Computing Technologies
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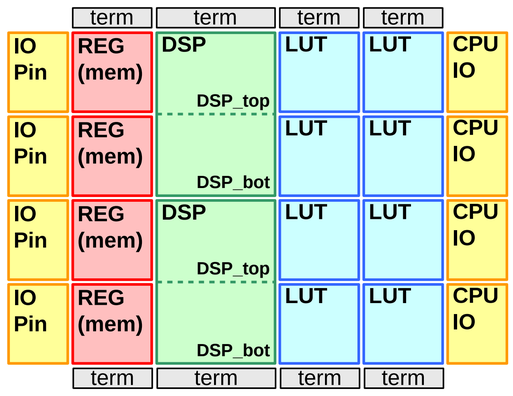
Gefördert durch:
Bundesministerium für Forschung, Technologie und Raumfahrt

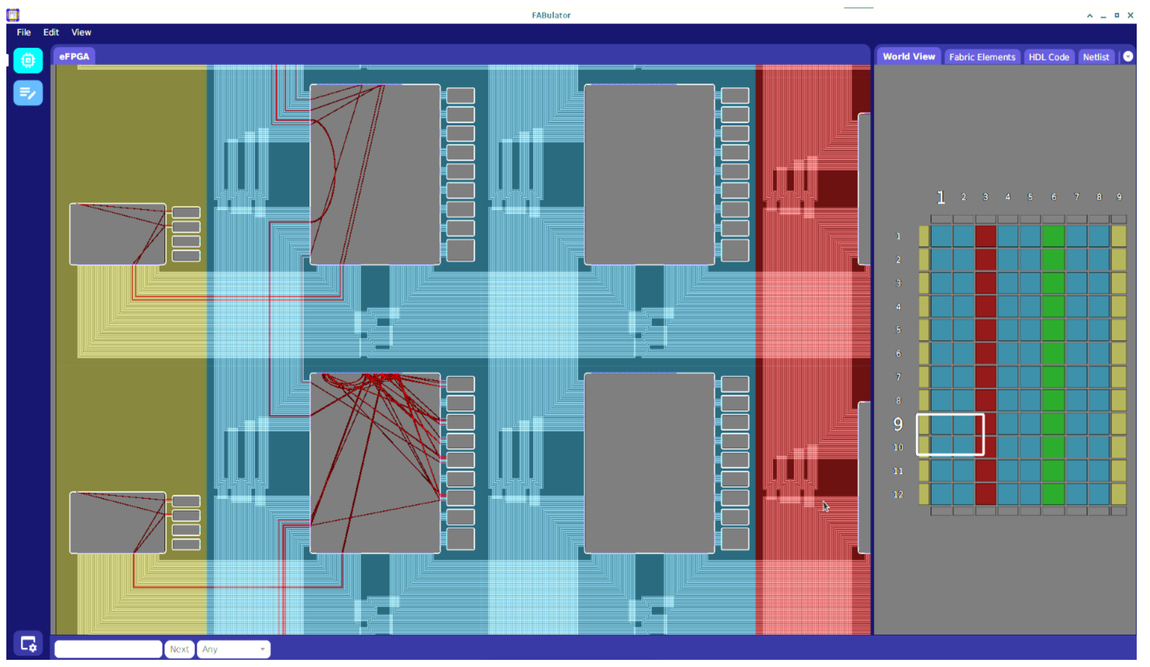
The FABulous Ecosystem

- Fully integrated open-source FPGA framework with good quality of results (area & performance)
  → can achieve >95% core density
- Entirely open and free, including commercial use (FABulous integrates many other projects)
- Supports custom cells, e.g., pass-gate multiplexer
- Example tiles for logic (LUTs), Block-RAM and DSPs
- Supports partial reconfiguration
  (supported in the fabric and by the design tools)
- Designed for ease of use while providing full control as needed
- Versatile
  - LibreLane ←→ Cadance and Yosys/nextpnr
  - Easy to customize, incl. the integration of own IP
  - Verilog and VHDL code generation
  - Flexible architecture modelling
  - Frame-based versus and shift register configuration

- Documentation:
  https://fabulous.readthedocs.io/en/latest/



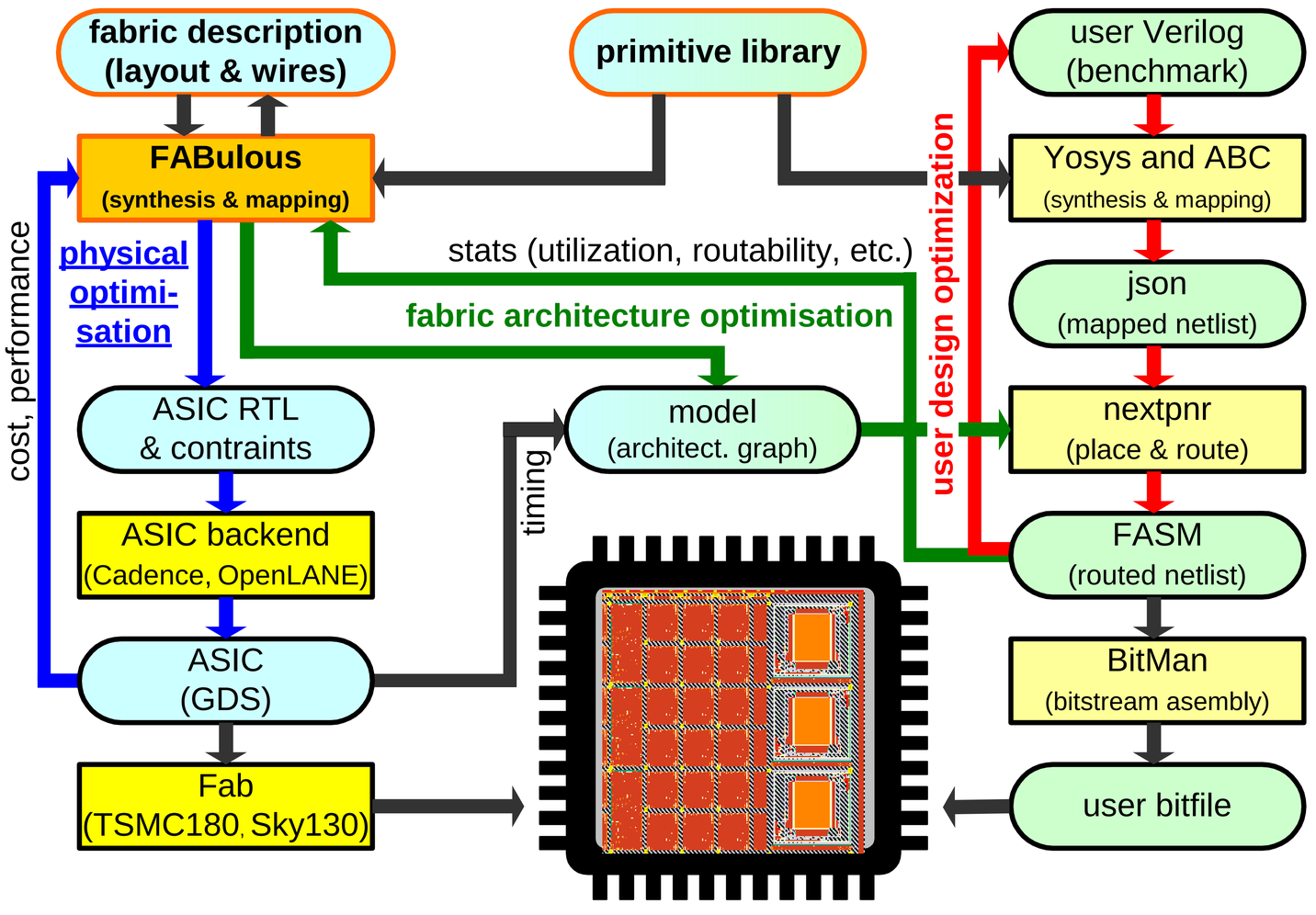
	A	B	C	D	E	F
1	*FabricBegin*					
2	NULL	N_term	N_term	N_term	N_term	NULL
3	W_IO	RegFile	DSP_top	LUT4AB	LUT4AB	CPU_IO
4	W_IO	RegFile	DSP_bot	LUT4AB	LUT4AB	CPU_IO
5	W_IO	RegFile	DSP_top	LUT4AB	LUT4AB	CPU_IO
6	W_IO	RegFile	DSP_bot	LUT4AB	LUT4AB	CPU_IO
7	NULL	S_term	S_term	S_term	S_term	NULL
8	*FabricEnd*					



Used PDKs

- TSMC
  180, 130, 55, 28
- Global Foundries
  180*, 22 FDX
- Skywater **130***
- IHP*
  - **130 BiCMOS***
  - **SG13CMOS5L***
- XFAB 180nm
  (sensor process)

Together >25 tapeouts with a FABulous fabric

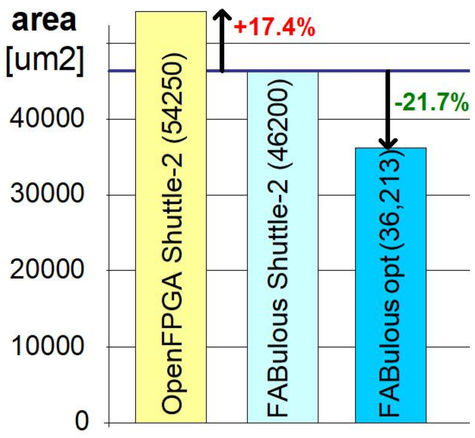


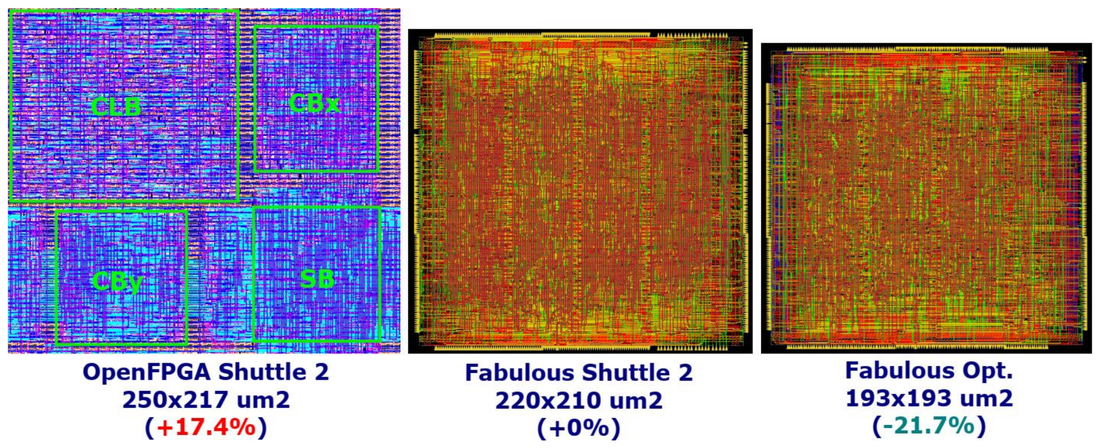
The FABulous Ecosystem

- ASIC generation
  - ASIC RTL code generation
  - Constraints generation
  - Open-source and industry tool support
- Simulation/Emulation
  - RTL simulation (Verilator or industry simulator)
  - Emulation on FPGAs (hard-annotate bitstream)
- RTL to bitstream compilation
  - Based on Yosys and nextpnr (optional VPR)
  - Models are automatically kept in sync
  - Timing driven place & route
  - Support for custom primitives
  - Same bitstream for simulation, emulation and ASIC
- Design for manufacturability
  - Test bitstream for ASIC production test
  - On-silicon timing characterization

FABulous Advantages

- Best open-source FPGA framework with respect to:
  - Area (~40% less area than openFPGA on Sky130)
  - Only framework supporting partial reconfiguration
  - Only framework using cheap configuration latches
  - Most versatile (supported tools and fabric modelling)
- FPGA 2021 “FABulous: An Embedded FPGA Framework”
- FPGA 2022 “How to Shrink My FPGAs”

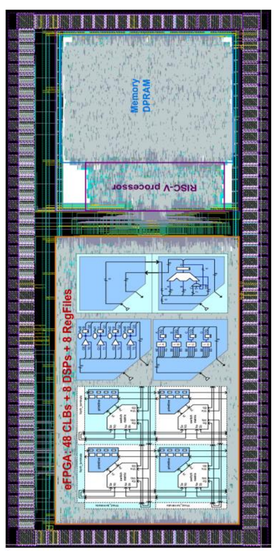




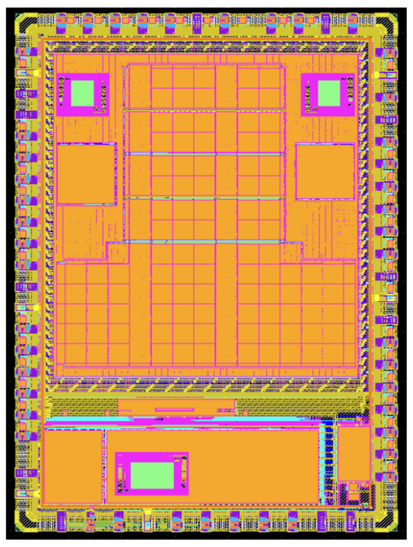
OpenFPGA Shuttle 2
250x217 um2
(+17.4%)

Fabulous Shuttle 2
220x210 um2
(+0%)

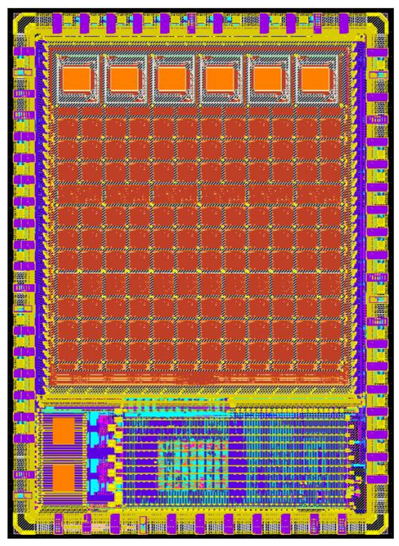
Fabulous Opt.
193x193 um2
(-21.7%)



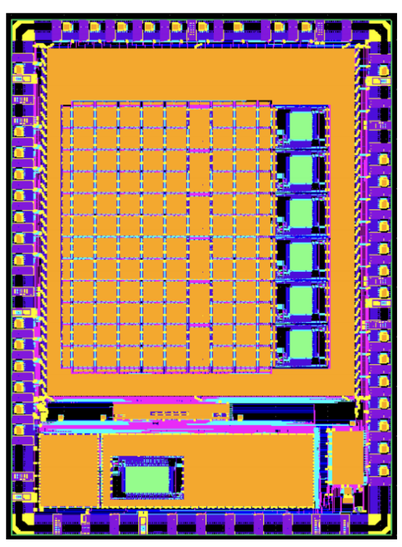
eFPGA_RISCV
Ibex-eFPGA
TSMC 180



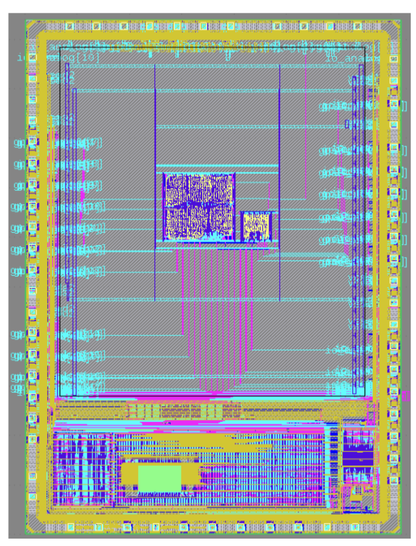
ICESOC_caravel
Ibex-Crypto-eFPGA
Skywater130



eFPGA_caravel_sky130
CLBs, DSPs, RegFiles,
BRAMs (custom muxes)



Open-Everything FPGA
(no industry tools)
Skywater130



ReRAM eFPGA
non-volatile eFPGA
Skywater130

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Find our repos under:
github.com/FPGA-Research