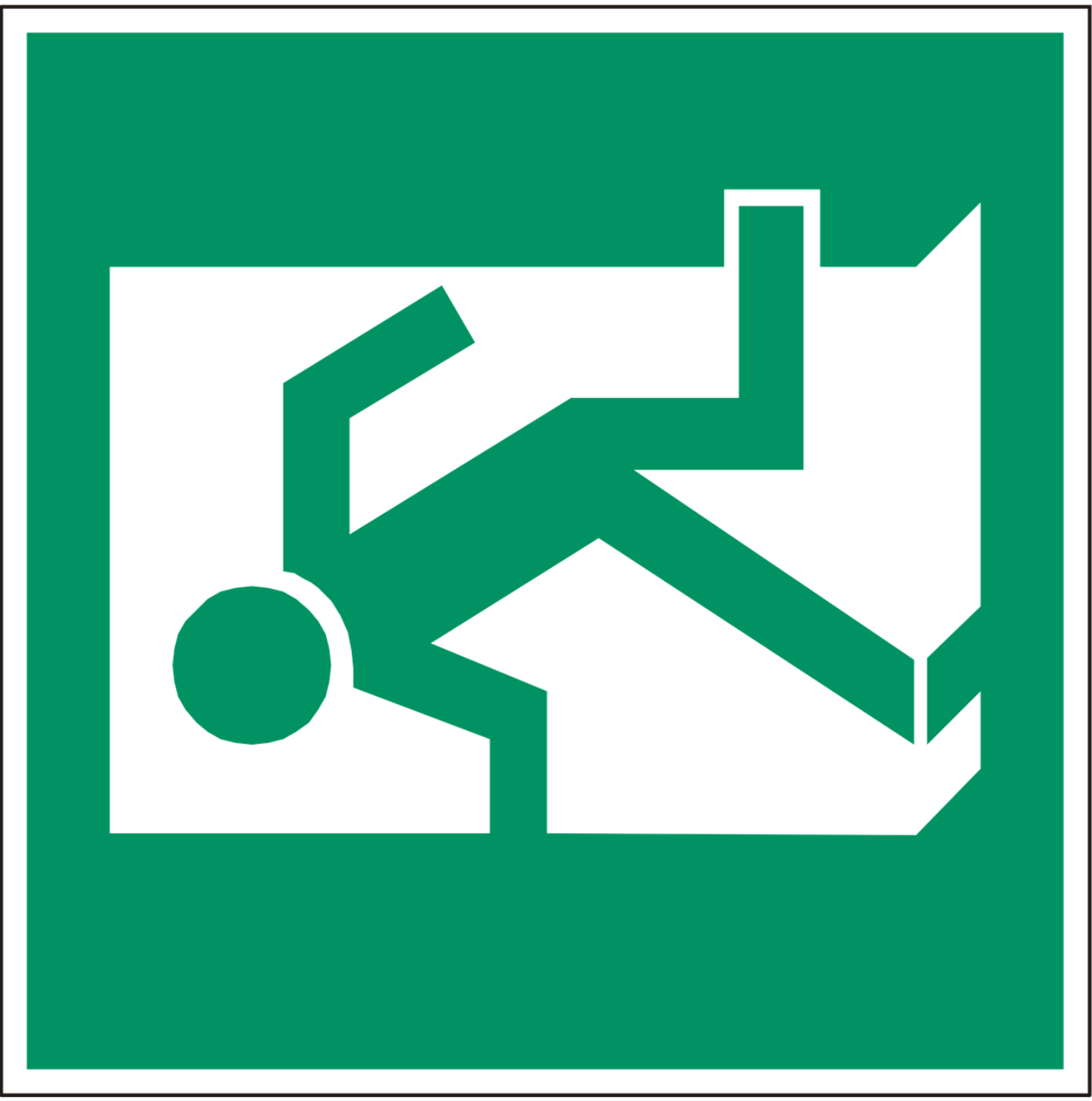
https://heichips.github.io/

Source: https://pixabay.com/users/openicons-28911/



UNIVERSITÄT
HEIDELBERG
ZUKUNFT
SEIT 1386


A.F. Thibaut

Our Venue

European Institute for Neuromorphic Computing (EINC) research building

Building tours will be available on

Tuesday and Wednesday

Electrons —
Spiking
Neuromorphic Hardware

Photons —
Highly-integrated
Neuromorphic Optics

Atoms —
Ultracold Quantum
Simulators

Our Sponsors

Gefördert durch:

Bundesministerium
für Forschung, Technologie
und Raumfahrt

Federal Ministry
of Research, Technology
and Space

Don‘t hesitate to sponsor us next year!

DE:SIGN | R&D PROJECTS OPEN SOURCE EDA TOOLS

Talents: Student contest „Open Source Chip Design Challenge“ (**OCDCpro**)

Analog design

- ✓Text based design (**ORDeC**)
- ✓High frequency chips (**DEMICO**)

Hardware security

- ✓HW architecture (**ExViPaS**)
- ✓HW security module (**SIGN-HEP**)

Digital design

- ✓eFPGAs (**OWAS**)
- ✓FPGAs (**FEntWumS**)
- ✓RISC-V (**GATE-V**)
- ✓Verifaction (**OSVISE**)
- ✓DRAM (**DERAMSys**)
- ✓AI Hardware (**EDAI**)

Novel technologies

- ✓RFETs (**ReDesign**)
- ✓MEMS/ASIC (**Meta-X**)
- ✓Packages/SiP (**PASSIONATE**)
- ✓Radiation resistant HW (**Flowspace**)

https://www.elektronikforschung.de/foerderung/bekanntmachungen/foerderaufruf-2025-deutschland-taiwan

Förderaufruf 2025 zur Rahmenrichtlinie zur Förderung der Forschungs- und Innovationszusammenarbeit mit Taiwan auf dem Gebiet der Mikroelektronik

Dieser Förderaufruf nimmt Bezug auf die Rahmenrichtlinie zur Förderung der Forschungs- und Innovationszusammenarbeit mit Taiwan auf dem Gebiet der Mikroelektronik vom 9. Juli 2024 (Bundesanzeiger vom 19. Juli 2024).

EINREICHUNGSFRIST

01.07.2025 - 01.10.2025

KONTAKT

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NEWSLETTER

In unserem Newsletter informieren wir Sie anlassbezogen über aktuelle Bekanntmachungen, Veranstaltungen und Meldungen aus der Forschungscommunity.
→ Zur Anmeldung

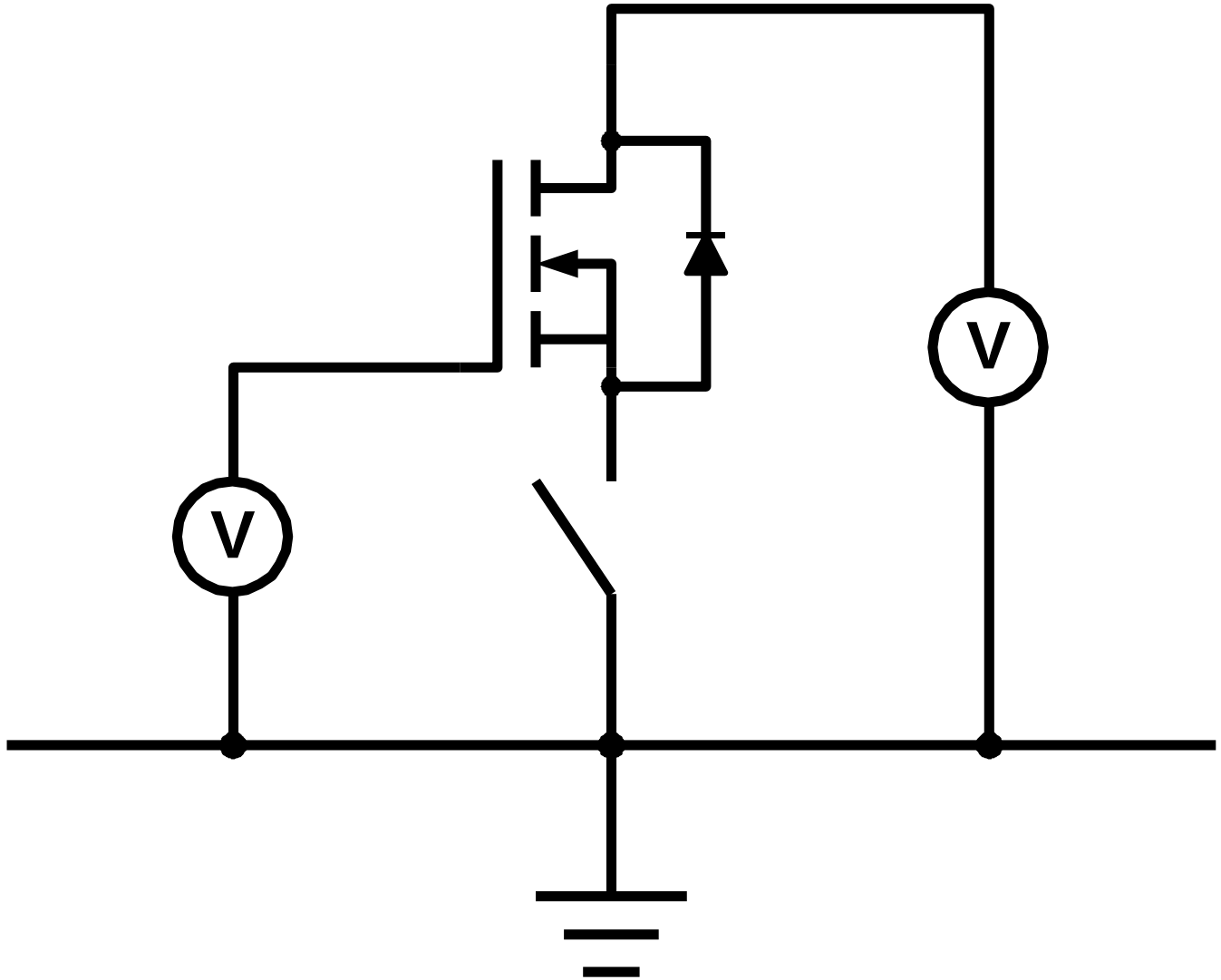
CHATBOT

Our Group: Novel Computing Technologies

UNIVERSITÄT HEIDELBERG
ZUKUNFT SEIT 1386

- FPGA CAD Tools
- Partial Reconfiguration
- Reliability
- Applications
- eFPGAs
- Hardware Security
- 16K RISC-V Threads on a single FPGA

Virtually everything we use and build during HeiChips is or will be…



Day 1 (Monday, August 4th)

9:30 Reception and refreshments

10:00 – 10:30 **HeiChips 2025 opening and program introduction**

10:30 – 11:30 **Poster Pitches**

11:30 – 12:00 **Poster networking coffee**

12:00 – 12:45 GreyHound (Leo Moser) KeyNote

12:45 – 14:00 Lunch

14:00 – 14:45 Keynote Jennifer Hasler Abstract

14:45 – 15:10 Coffee break

15:10 – 15:55 Keynote Veena S. Chakravarthi "Smarter Chips, Healthier Lives" Abstract

16:00 Hike to Neuburg Abbey (over the Philosophers' Walk) and dinner (18:00) at Klostergarten

Day 2 (Tuesday, August 5th)

8:45 – 9:00 Reception and refreshments

9:00 – 10:30 Kickoff (15 min, Dirk) (15 min max) & Class (Jennifer Hasler)
Analog Design and Floating-gate Technology

10:30 – 11:00 Coffee break

11:00 – 12:30 Lab (Jennifer Hasler)

12:30 – 13:30 Lunch

13:30 – 15:00 Class (Krzysztof)
Open-source process design kit based on IHP-SG13G2 technology

15:00 – 15:30 Coffee break

15:30 – 17:00 Lab (Krzysztof) A review of template designs exploring IHP-Open-PDK views and components

19:00 Dinner at Brauhaus Vetter and city tour.

Vetter33 was the strongest beer in the world in the Guinness Book of Records in 1994

Day 3 (Wednesday, August 6th)

8:45 – 9:00 Reception and refreshments

9:00 – 10:15 Class Stefan Wallentowitz "Build your logic design tool with CIRCT"

10:15 – 10:45 Coffee break

10:45 – 12:00 Lab Stefan Wallentowitz and Tobias Wölfel Lab on CIRCT

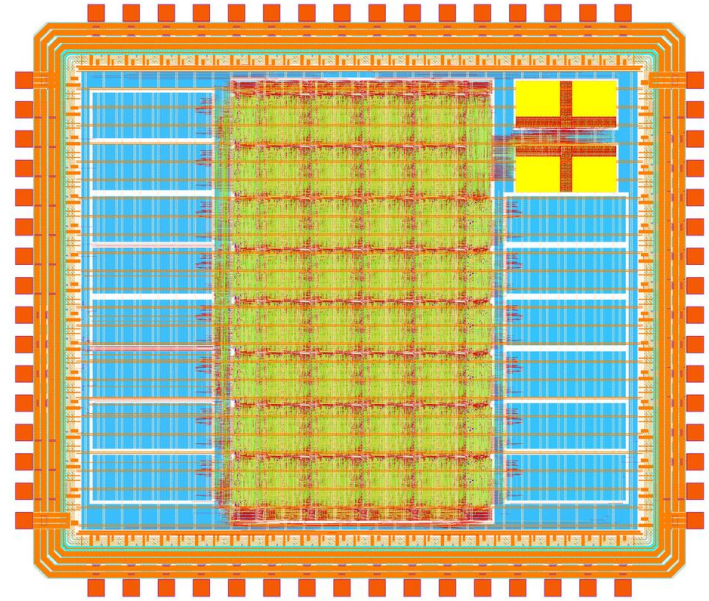
12:00 – 13:00 Lunch

13:00 – 14:30 Class (Leo Moser) "LibreLane"
This class provides an introduction to LibreLane, its architecture and usage, as well as an overview of a typical digital design flow in general.

14:30 – 15:00 Coffee break

15:00 – 17:00 Lab (Leo Moser) "LibreLane"
In this Lab, you will get hands-on practice using LibreLane to design ASICs with an open-source PDK in preparation for the hackathon.

Day 4 (Thursday, August 7th)



Hackathon

8:45 – 9:00 Reception and refreshments

9:00 – 10:00 Talk and Hackathon Kickoff

10:30 – 11:00 Coffee break

11:00 – 12:30 Hackathon (RTL -> Silicon)

12:30 – 13:30 Lunch

13:30 Hackathon (RTL -> Silicon)

Day 5 (Friday, August 8th)

Hackathon

8:45 – 9:00 Reception and refreshments

9:00 – 16:30 Hackathon

16:30 Best Project Award and Wrap-Up

- **Implantable-compatible transceiver designed for tissue-coupled data transfer**
- **Wearable health sensor**
- **Cryogenic detector and conducting qubit readout and control logic**
- **Something I could legitimately show off to my neighbor downstairs**
- **Different SRAM blocks or … differential current mode logic**
- **Open-everything SoC with eFPGA (new FABulous architecture?)**
- **Temperature sensor that uses an on-chip diode**
- **Various ML accelerators (DNN, Spiking/Neuromorphic, Tsetlin Machine)**
- **PV maximum power point tracking**

You can help us

- We plan an open-everything

  RISC-V + eFPGA Hybrid (like a simple

  ZYNQ-style chip

- Will provide microcontroller RISC-V
- eFPGA with ~1K LUTs
- Debug infrastructure, tutorials, demos

- Memory subsystem
- HDMI output (or even input?)
- Delay block (or even a DLL/PLL)
- Fast IOs, SRAM, Fuses, …

https://heichips.github.io/