A tiny systolic array (4x4)

HeiChips 2025 summer school workshop

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What are we making ?

A 4x4 output stationary systolic array

- Computes the product of two 4x4 matrices
- Each input matrix element is a 4-bit unsigned integer
- Addition is performed in 8 bits

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Why ?

- Widely used in NN hardware accelerators
- Highly parallel
- Intermediate results are stored within the array

The output stationary systolic array

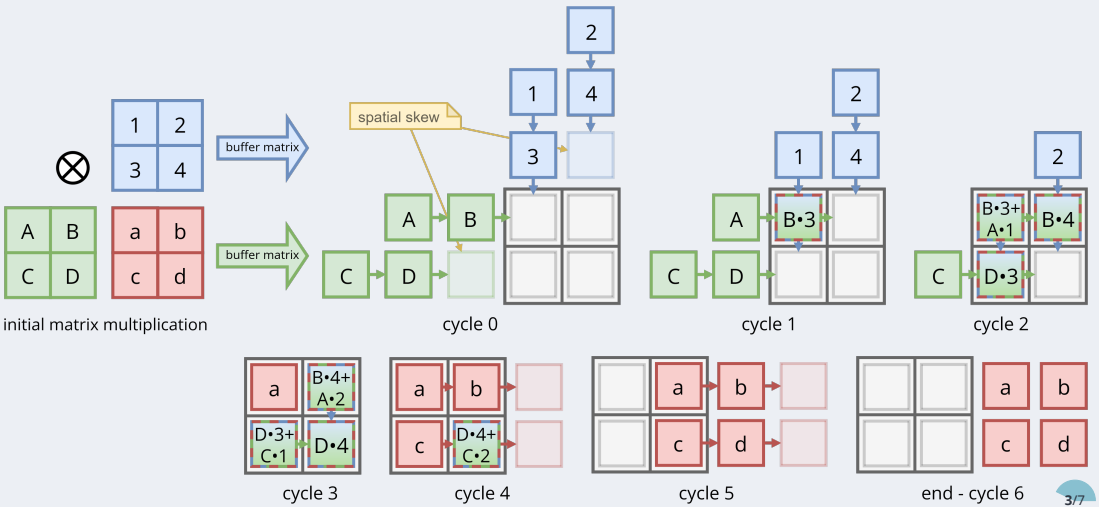
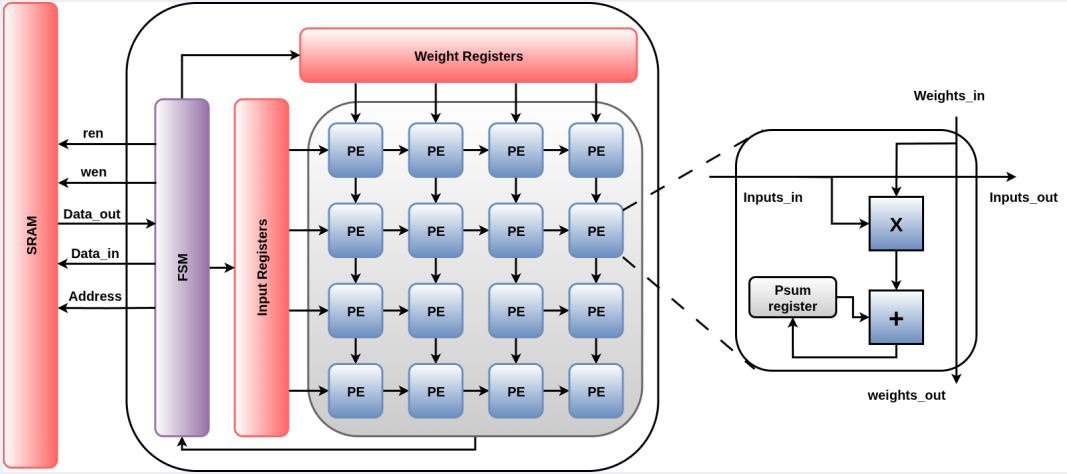
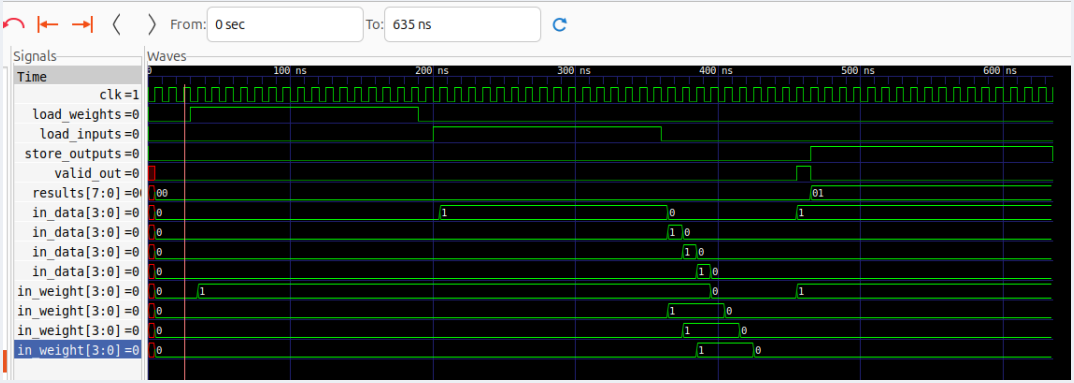


Figure: Image courtesy of EMJzero from Wikimedia Commons

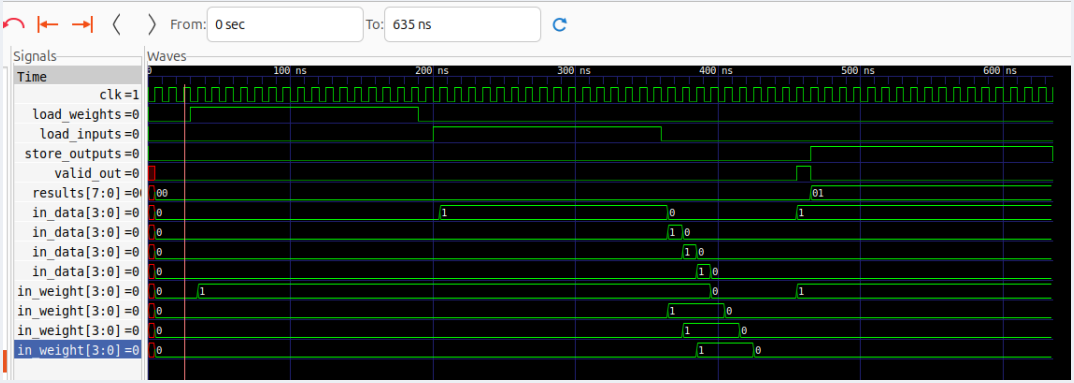
Hardware implementation



It works !


From: 0 sec
To: 635 ns
Signals
Waves
Time
clk =1
load_weights =0
load_inputs =0
store_outputs =0
valid_out =0
results[7:0] =0
in_data[3:0] =0
in_data[3:0] =0
in_data[3:0] =0
in_data[3:0] =0
in_weight[3:0] =0
in_weight[3:0] =0
in_weight[3:0] =0
in_weight[3:0] =0
0
100 ns
200 ns
300 ns
400 ns
500 ns
600 ns

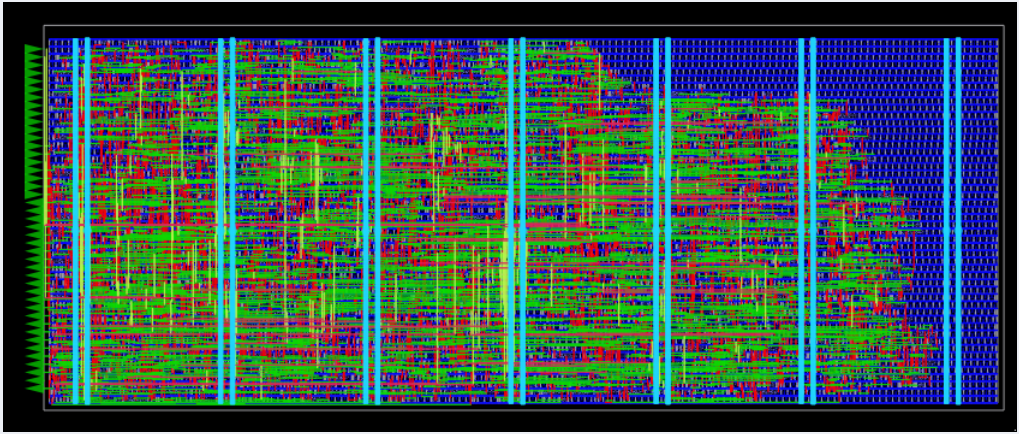
It works !



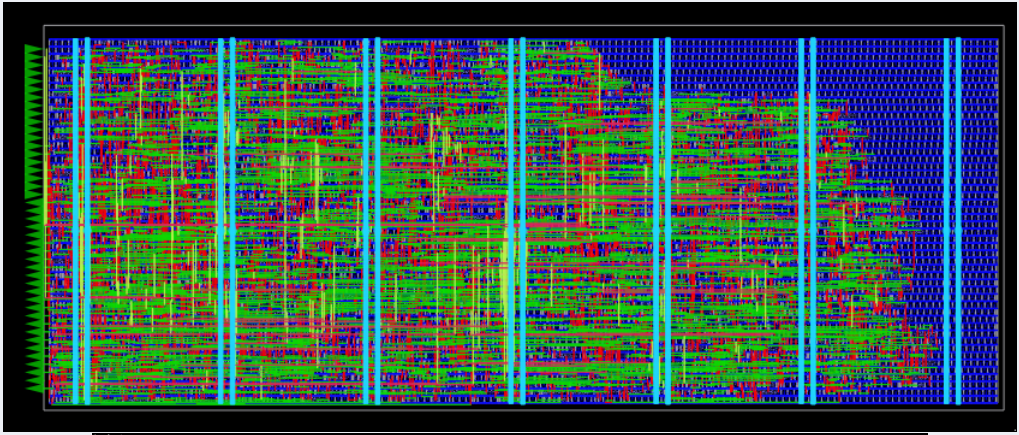
Tools

- Verilator
- Icarus Verilog

It works !



It works !



```
* Antenna
Passed ✔

* LVS
Passed ✔

* DRC
Passed ✔

[15:12:00] INFO     Saving views to                                          state.py:20
                    '/home/user/open_tools/heichips25_systolicArray4x4/librelane/runs/RUN_2025-08-08_14-56-15/fin
                    al …
[15:12:00] INFO     Flow complete.                                           sequential.py:41
```

Questions?