Open-source process design kit based on IHP-SG13G2 technology

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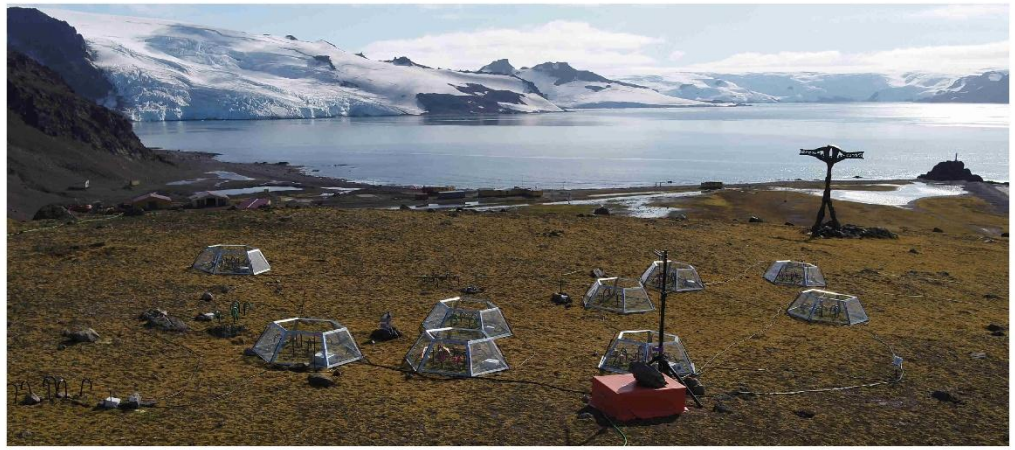
HeiChips, Heidelberg 2025

Projects: BMFTR -> FMD-QNC (16ME0831)

About me

- BSc in electronics
- MSc in Acoustics
- PhD in Telecommunications
- 15 years of experience in academia Poland/Chile
- bi-polar experience
- IHP-Open-PDK developer since 2023

...one of the first „victims” of the open-sourrce silicon movement



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IHP in a nutshell

- IHP is the European research and innovation centre for silicon-based systems, ultrahigh-frequency circuits and technologies,
- Unique selling point of a 200mm pilot line for state-of-the-art BiCMOS technologies, operated under industry-like conditions, 24/7, for the provision of prototypes and low-volume production runs.
- Qualified technological platform with direct access for science and industry
- Vertical structure from material research to system architecture
- 350+ employees, 40+ nationalities

Vision

"We create foundations and prototype applications based on future silicon-based technologies and systems for a digitalized and networked world as well as for the sustainable preservation of our natural living conditions."

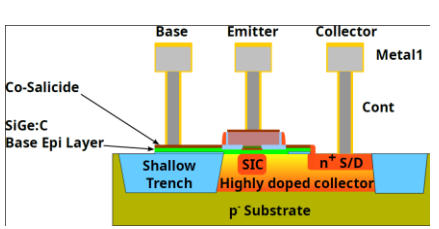
130nm SiGe BiCMOS Technologies for RF Applications

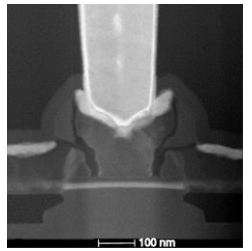
	SG13S	SG13G2	SG13G3Cu
HBT f_t / f_{max}	250 / 340 GHz	350 / 450 GHz	470 / 650 GHz
$W_{Emitter}$	170 nm	130 nm	110 nm
HBT BV_{CE0}	1.7 V	1.6 V	1.5 V
CMOS node	130 nm		
Active devices	Schottky diodes, Antenna diodes, PN diodes, ESD		
Varactors	NMOS Varactor		
HeiChipsors	Poly-Si, Thin Film		Poly-Si
MIM Caps	1.5 fF / µm² (Al) 2.1 fF / µm² (Cu)	1.5 fF / µm² (Al) 2.1 fF / µm² (Cu)	2.1 fF / µm²
Metallization	7 Layers AL incl. 2 & 3 µm layers or *Cu: 4 + 2 (3µm) Al: 2 (3µm)	7 Layers AL incl. 2 & 3 µm layers or *Cu: 4 + 2 (3µm) Al: 2 (3µm	*Cu: 4 + 2 (3µm) Al: 2 (3µm

*Cu BEOL from X FAB

- Target are high-end technology developments, low volume market introduction, technology transfer for potential mass production in commercial fabs
- SG13S & SG13G2 are qualified and ready for Low Volume of high end products
- SG13G3Cu is early access - qualification scheduled 2025

- SG13G2 technology was selected for the development of an open source PDK





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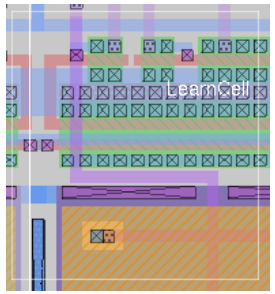
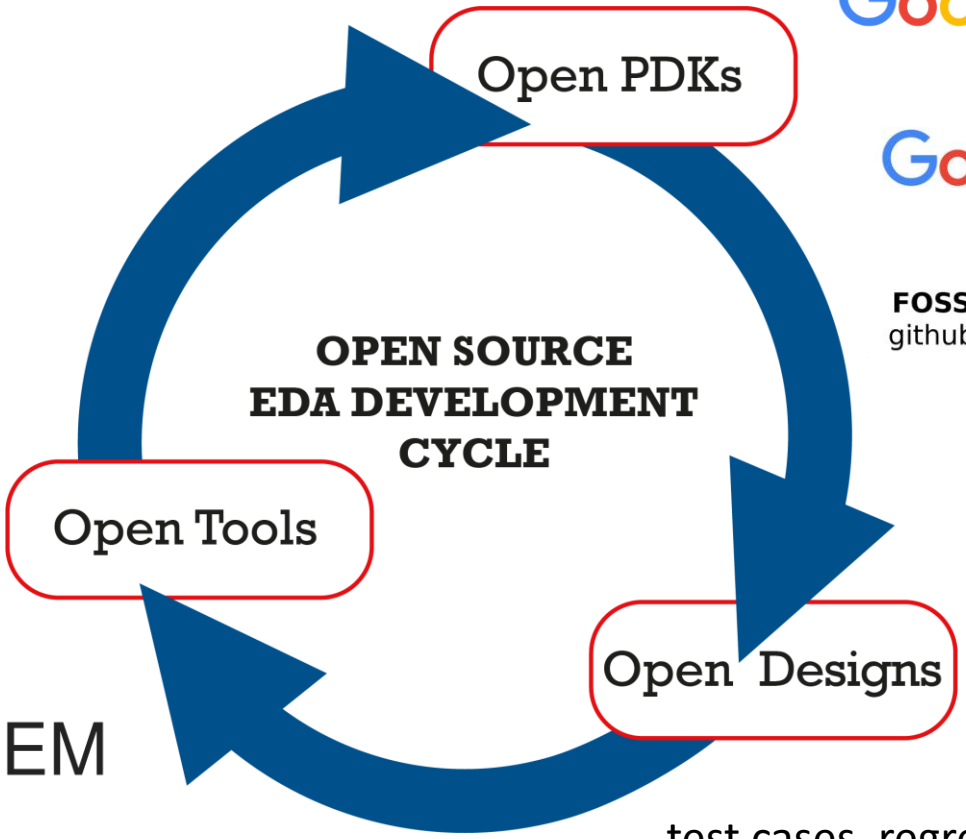
Open source ASIC development cycle



Qucs

NGSPICE

XSCHEM



Google + skywater TECHNOLOGY

Google + GLOBAL FOUNDRIES

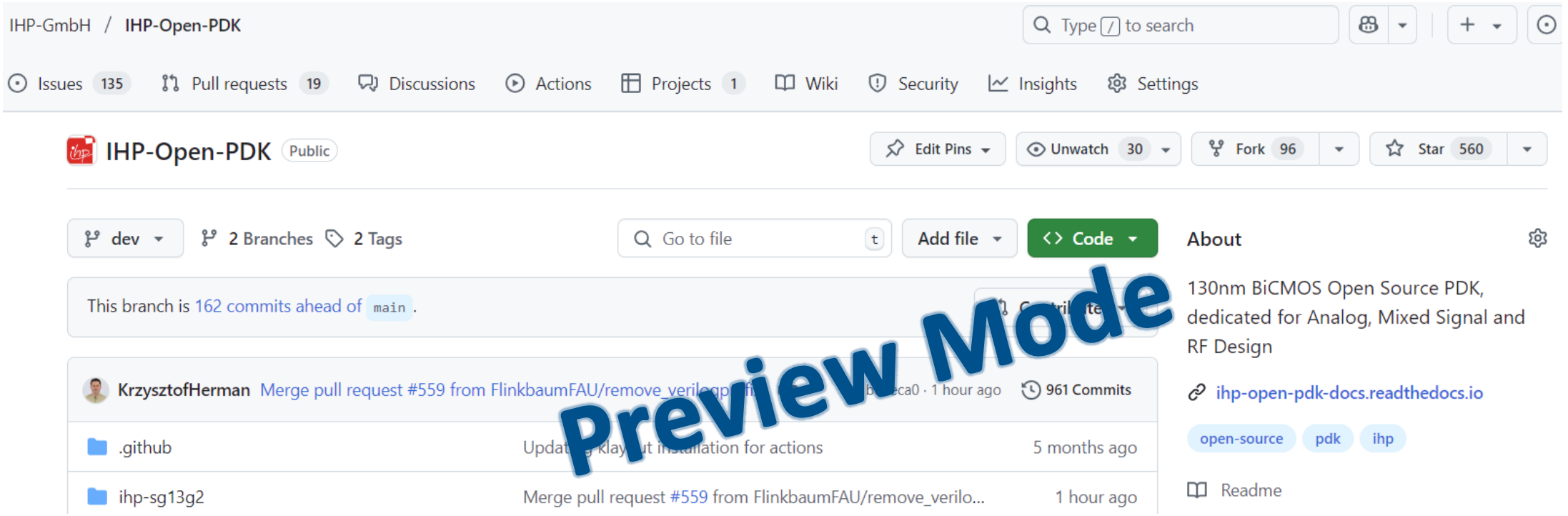
FOSS 180nm Production PDK
github.com/google/gf180mcu-pdk

IHP-Open-PDK

RISC-V®

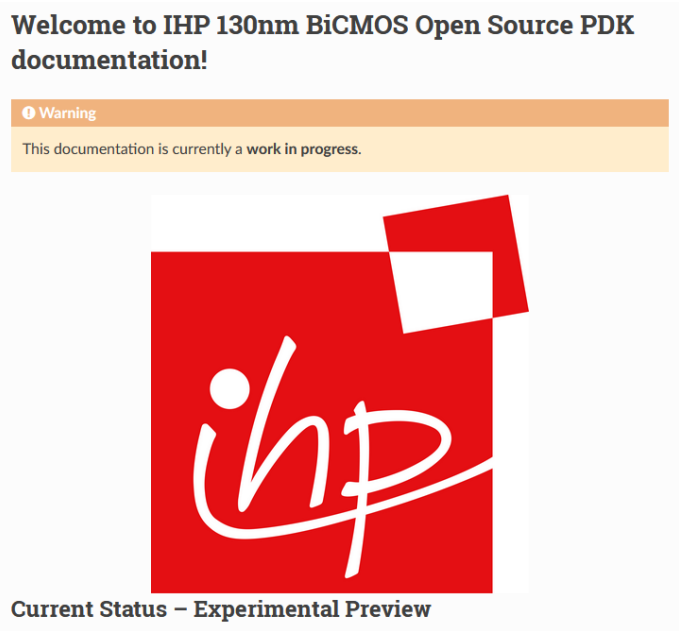
test cases, regression tests, benchmarks, use cases,
user stories, feedback, error reports, feature requests

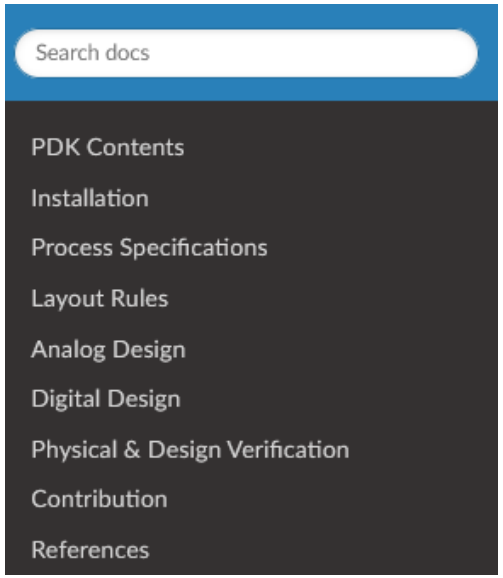
IHP Open PDK on github

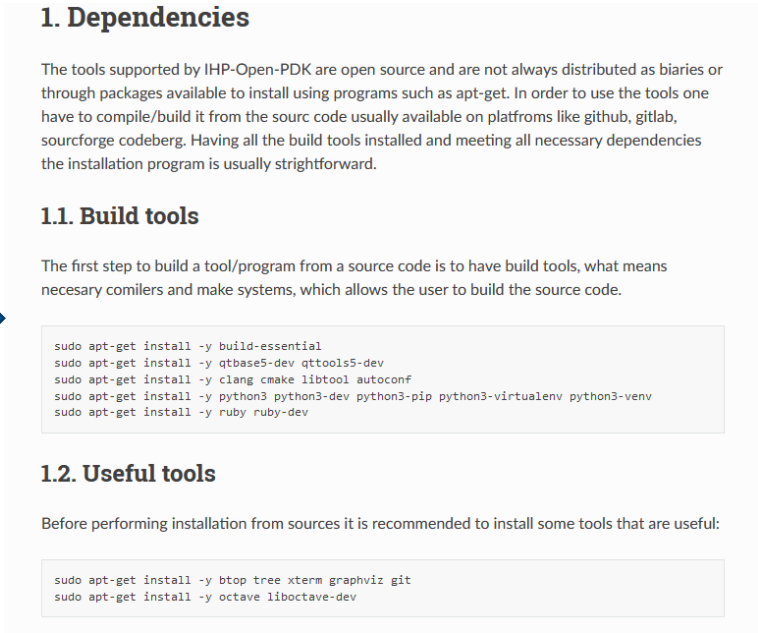


Minimal installation – plug and play & KISS approach

Working with the IHP Open PDK

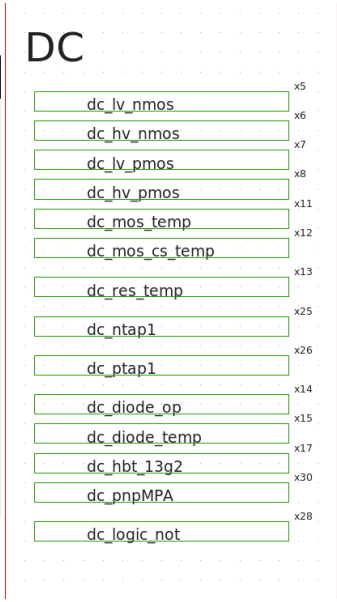


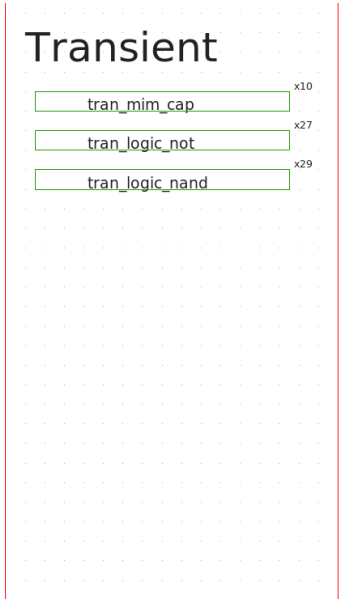


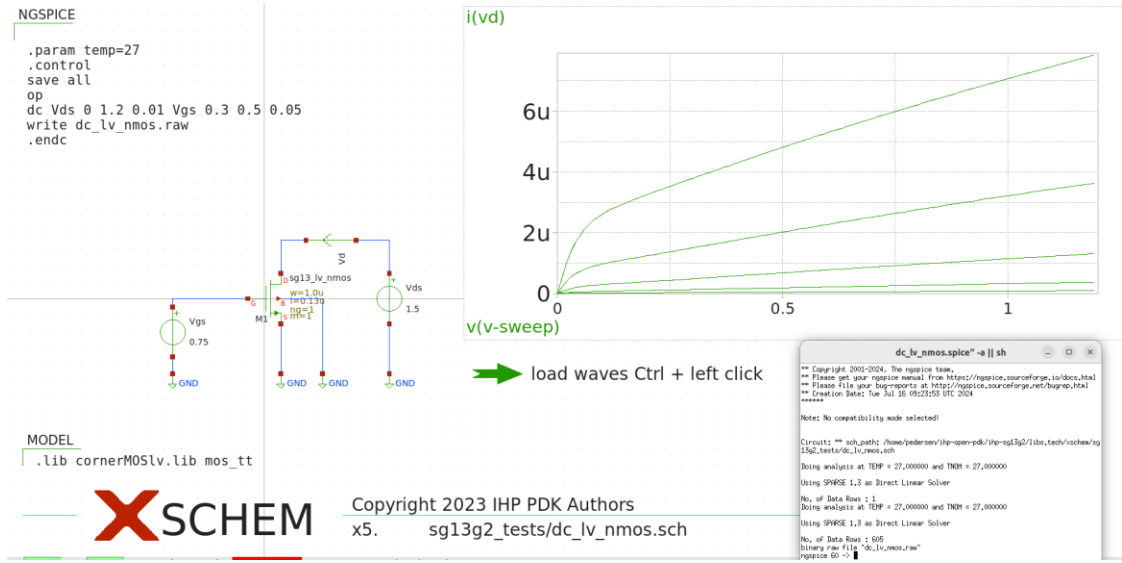


Ubuntu 22.04+ compatible
Configuration: $PDK_ROOT, $PDK
Dependencies installation: mainly apt-get
Tools have to be installed (binaries, sources)

Getting started really isn’t that hard!







Some of the Information Available in ChatGPT

1. Process Technology

- Overview of advanced semiconductor technology, including high-performance devices and integrated components
- Offers various modules for expanded functionality

2. Multi-Project Wafer (MPW) Services

- Includes details on pricing, schedules, and supported processes
- Specifies chip area requirements and approval process for smaller designs

3. Layout and Process Specifications

- Defines design rules, device specifications, and physical constraints
- Includes details on available materials and process layers

Design examples and courses

IHP-GmbH / IHP-AnalogAcademy

Code | Issues 32 | Pull requests | Actions | Projects

IHP-AnalogAcademy Private

main | 2 Branches | 0 Tags

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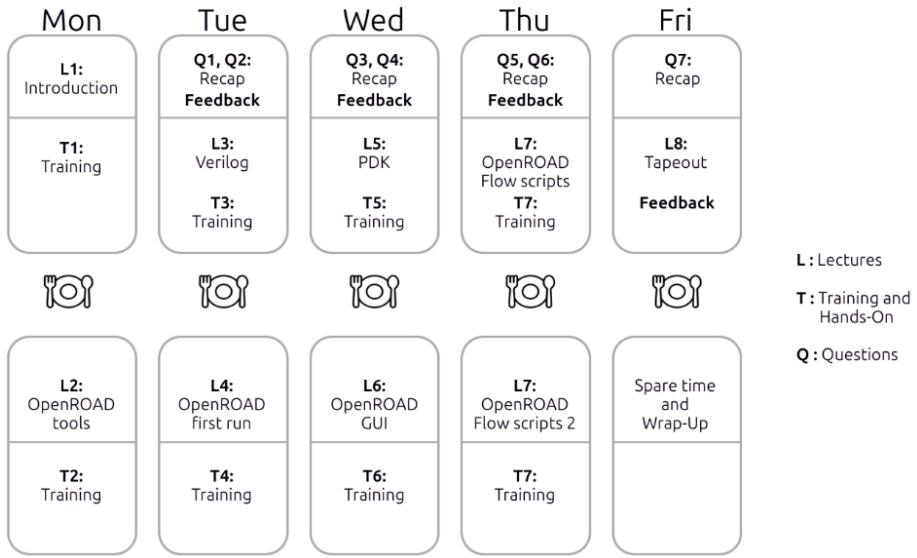
OS-EDA / Course

Code | Issues 3 | Pull requests | Projects | Wiki | Security | Insights

Course Public

main | 1 Branch | 10 Tags | Go to file

Course instance: 1 Week, hands on



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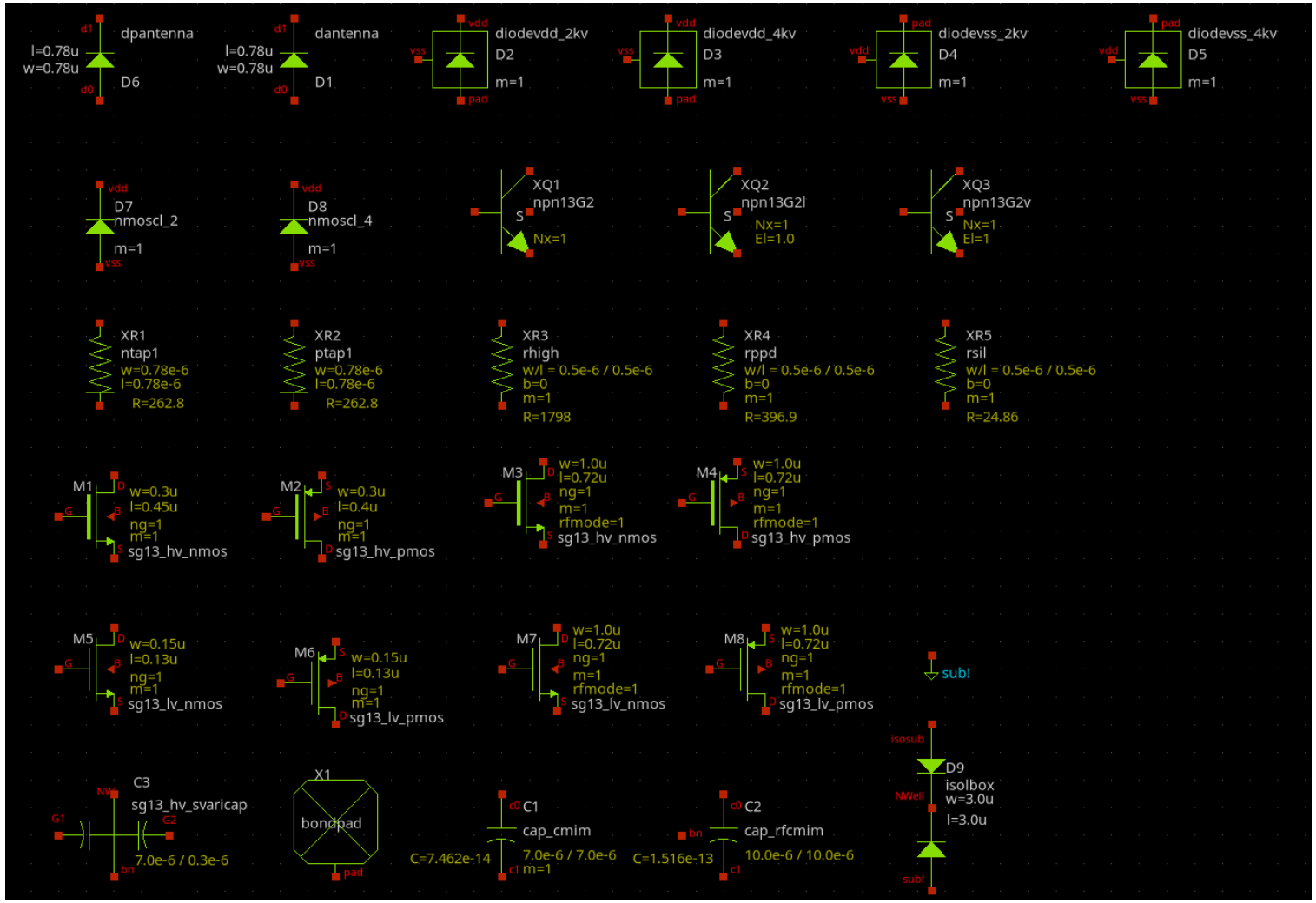
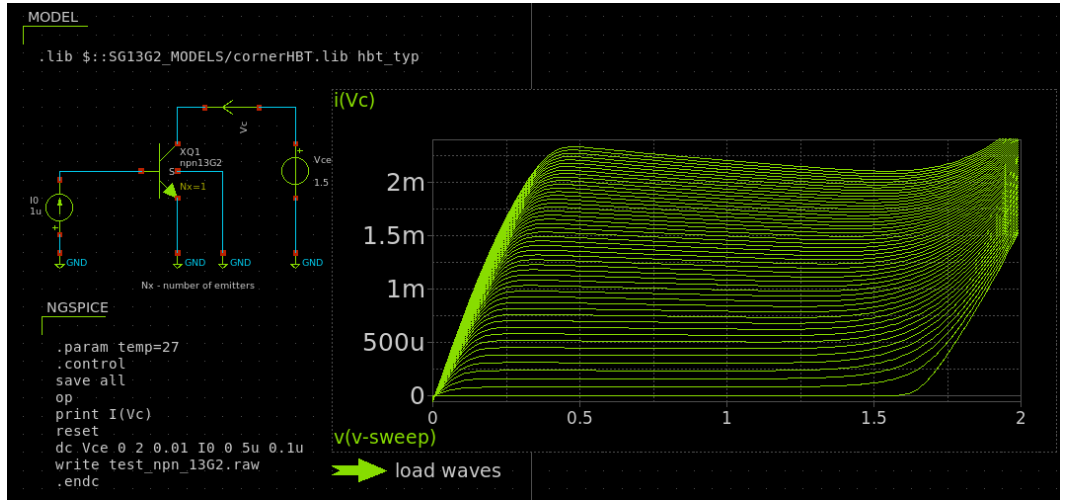
OpenPDK support for schematic capture

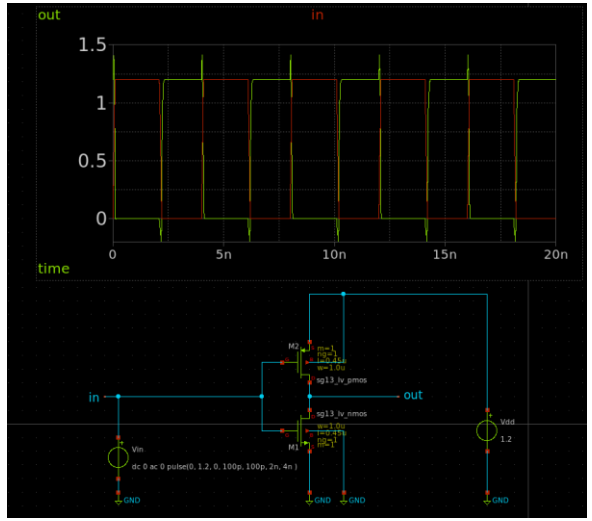


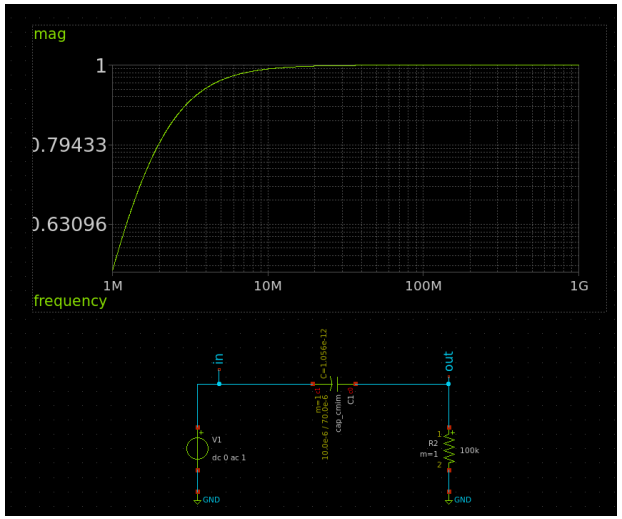
The current version of the IHP OpenPDK supports:

- xschem primitives for schematic capture
- automatic ngspice/Xyce compatible netlist generation
- example use cases to show the basic functionalities and parameters of the primitives

OpenPDK support for simulations



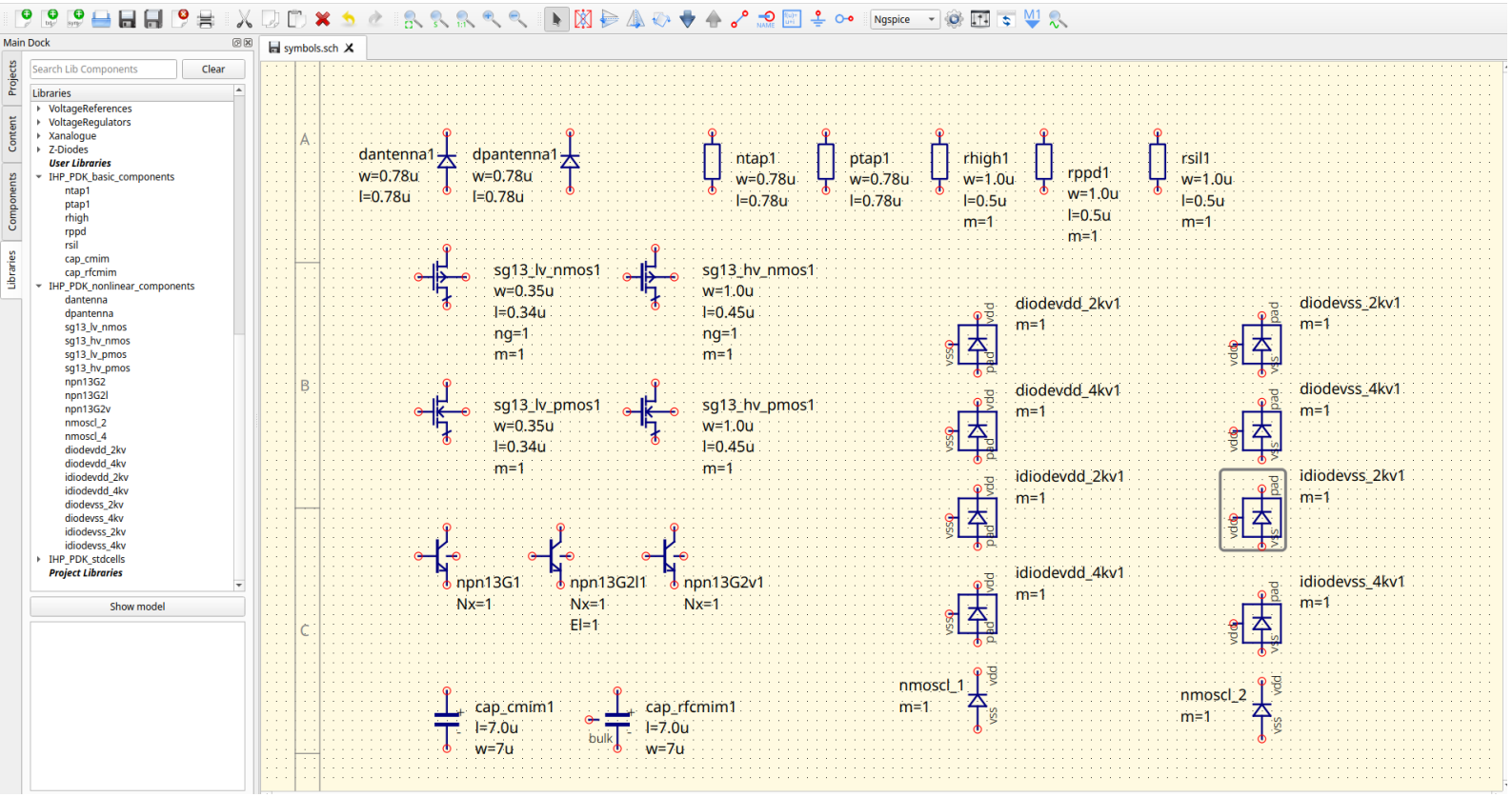




Analog simulation facilities:

- PSP103.6 MOSFET models from SemiMod,
- ngspice/Xyce compatible netlists,
- process corners: typical, best case, worst case,
- statistics related to the process variation,
- simulation examples segmented by simulation type: DC, TRAN, AC, MonteCarlo, S-parameters
- postprocessing python scripts,
- model extensions for RF frequency range,
- ngspice 40+ compatible

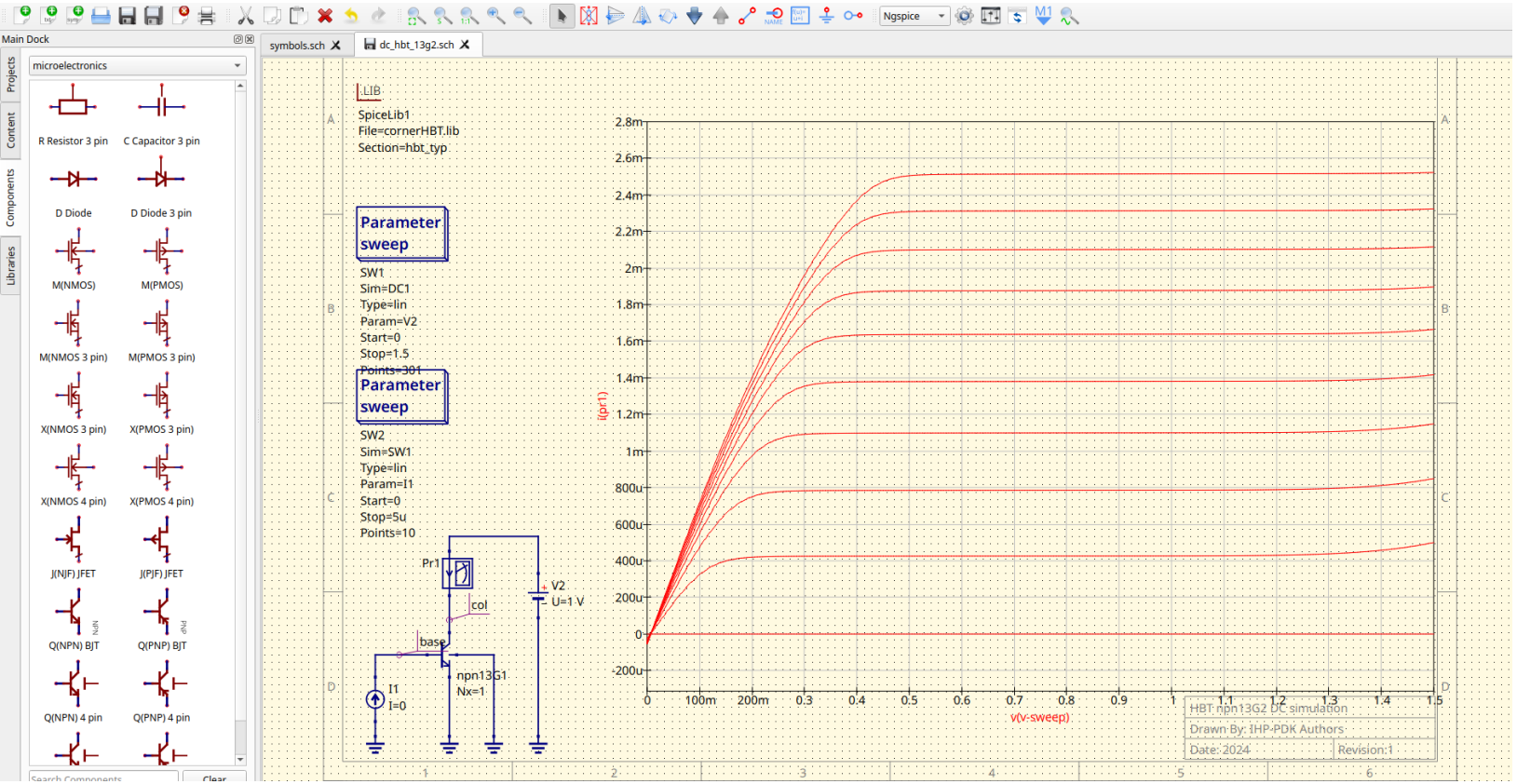
OpenPDK support for Qucs-S schematic capture



The current version of the IHP OpenPDK supports:

- primitives for schematic capture
- automatic ngspice/Xyce compatible netlist generation
- example use cases to show the basic functionalities and parameters of the primitives
- XSPICE model support (under development)

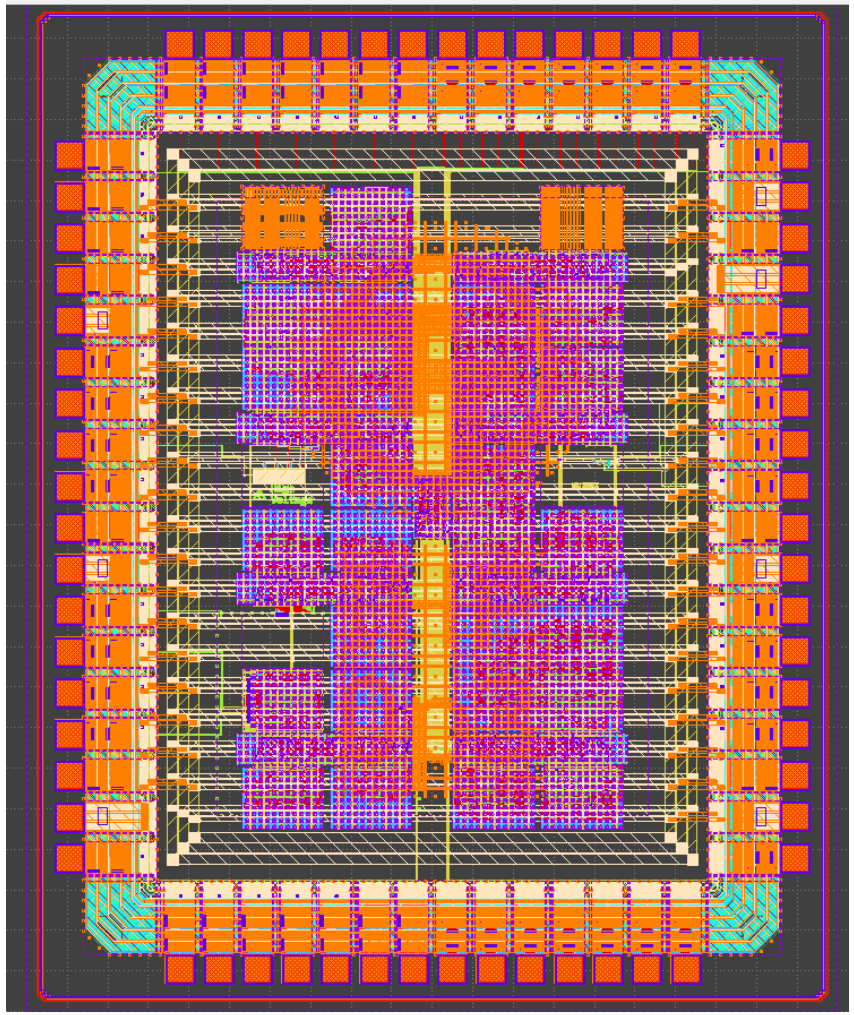
OpenPDK support for Qucs-S schematic capture

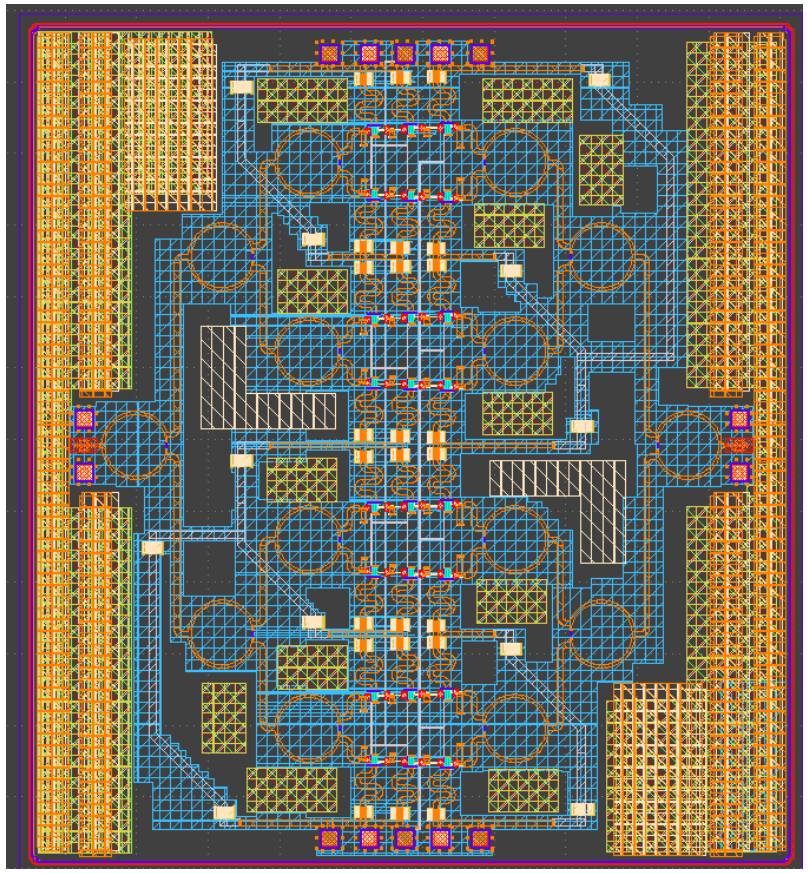


Qucs-S development:

- Agnostic support for PDK
- CDL netlisting
- Interoperability with OpenEMS and Klayout
- XML symbol library import
- RF related features

KLayout – primary tool for open source layout design

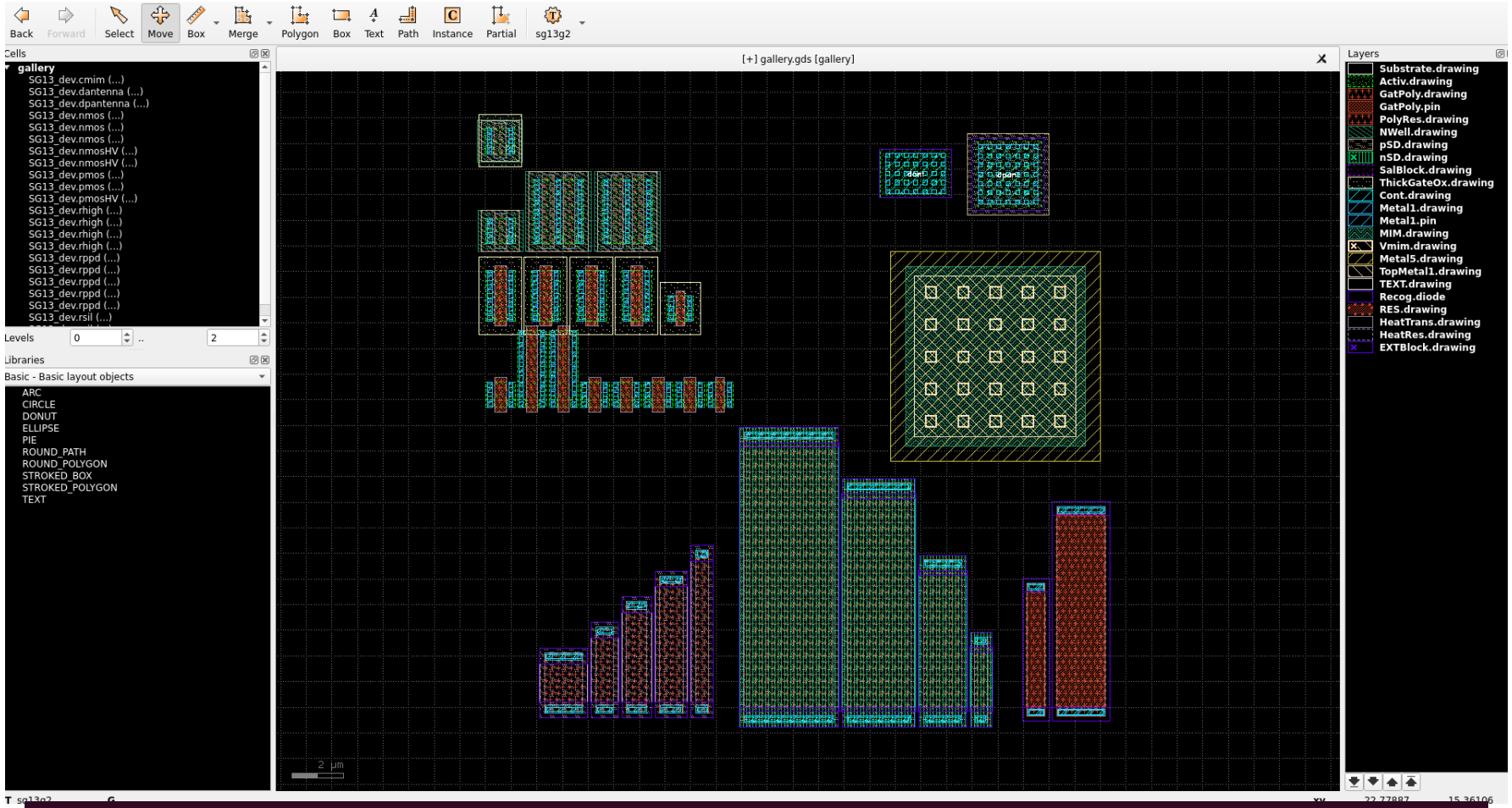




KLayout key features:

- hierarchical view
- parametric cell suport
- DRC/LVS checks
- command line batch mode
- XOR and DIFF tools
- Custom scripts in Python/Ruby
- Plugins

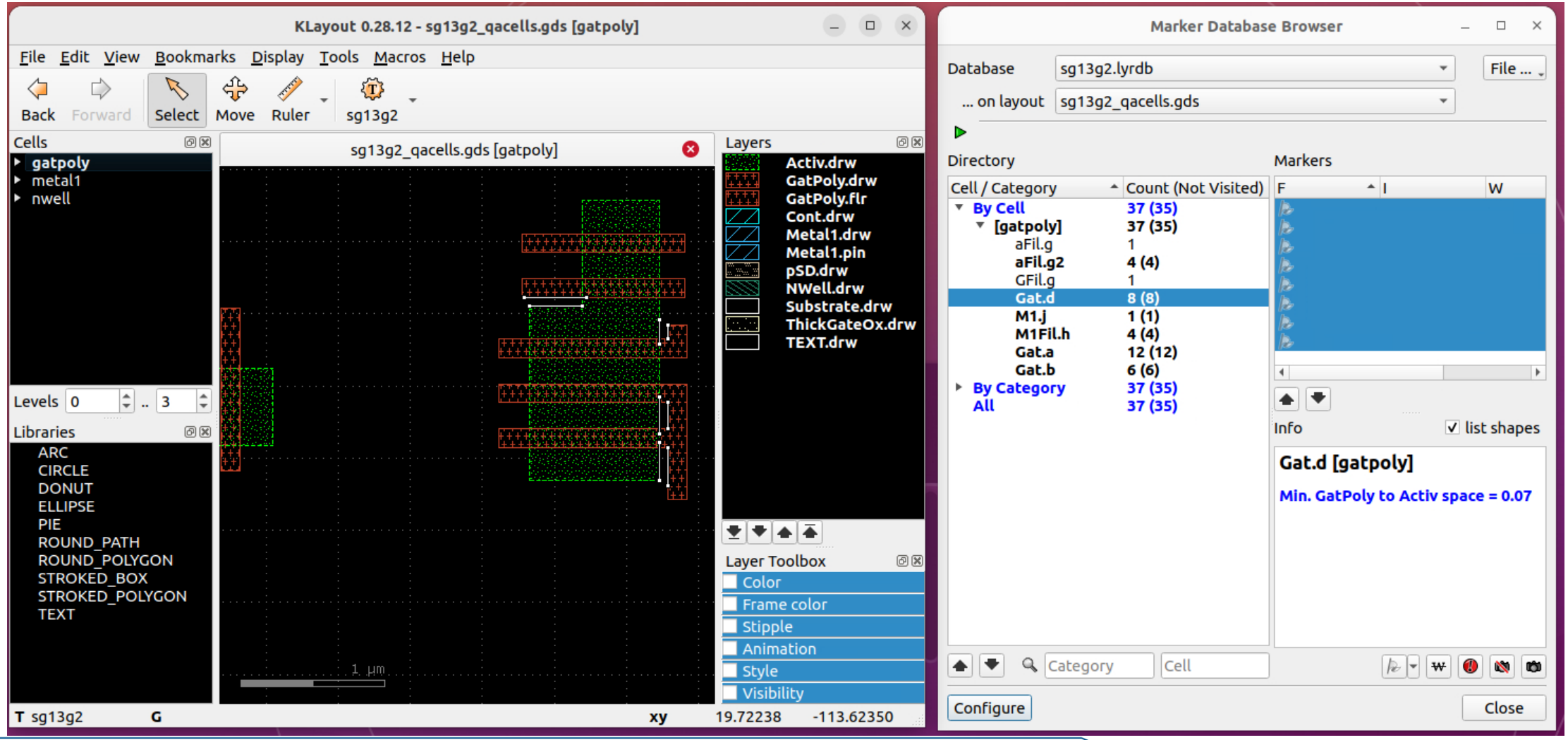
KLayout – Pycell support



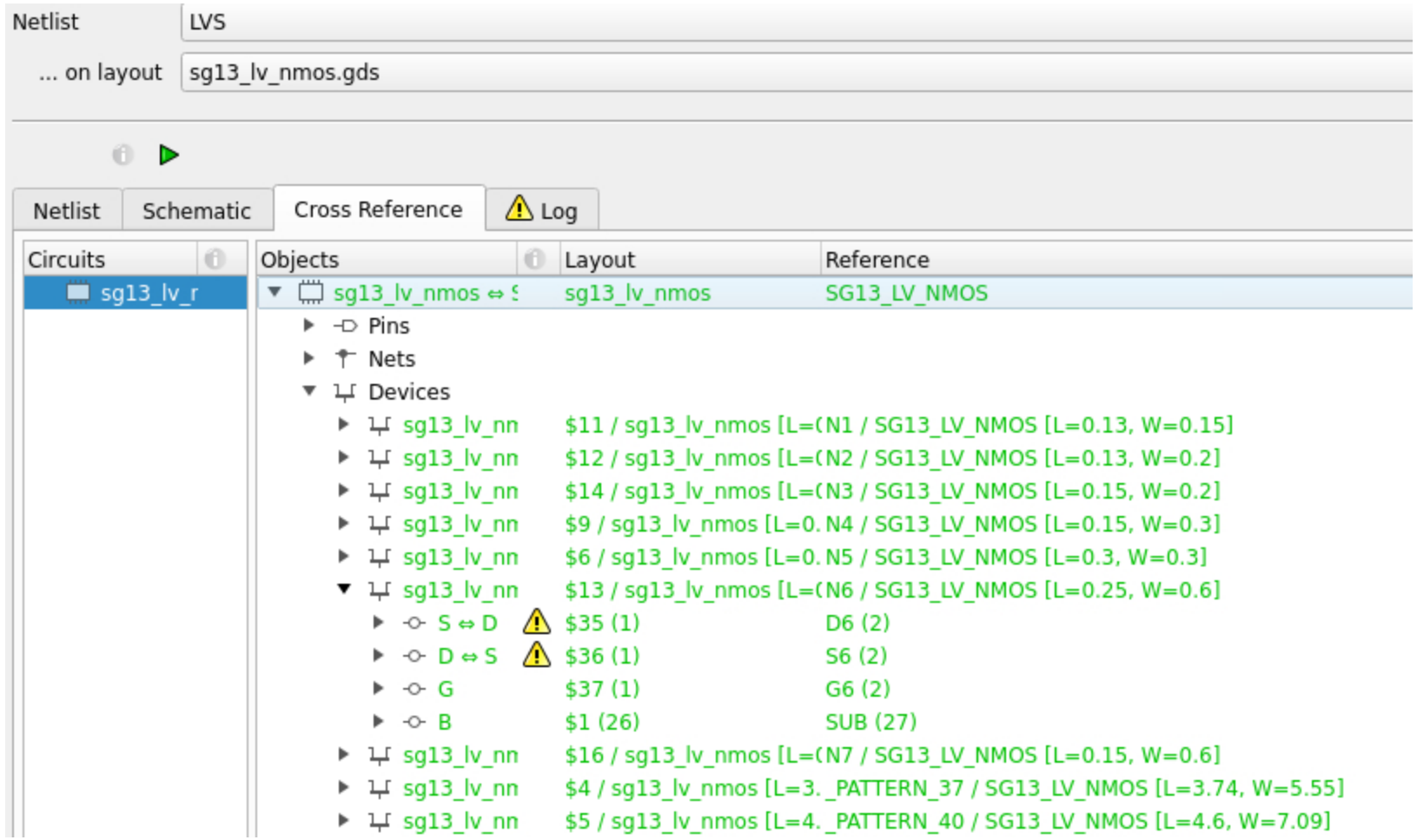
- Pycells compatible with Synopsys PyCell Studio and Keysight ADS
- KLayout wrapper API development
- Klayout Device generator

```
klayout -n sg13g2 -zz -r generator.py -rd netlist=netlist.spice -rd output=macros/gallery.gds
```

KLayout example DRC run on `gatpoly` QA cell



KLayout example LVS run on sg13_lv_nmos mosfets



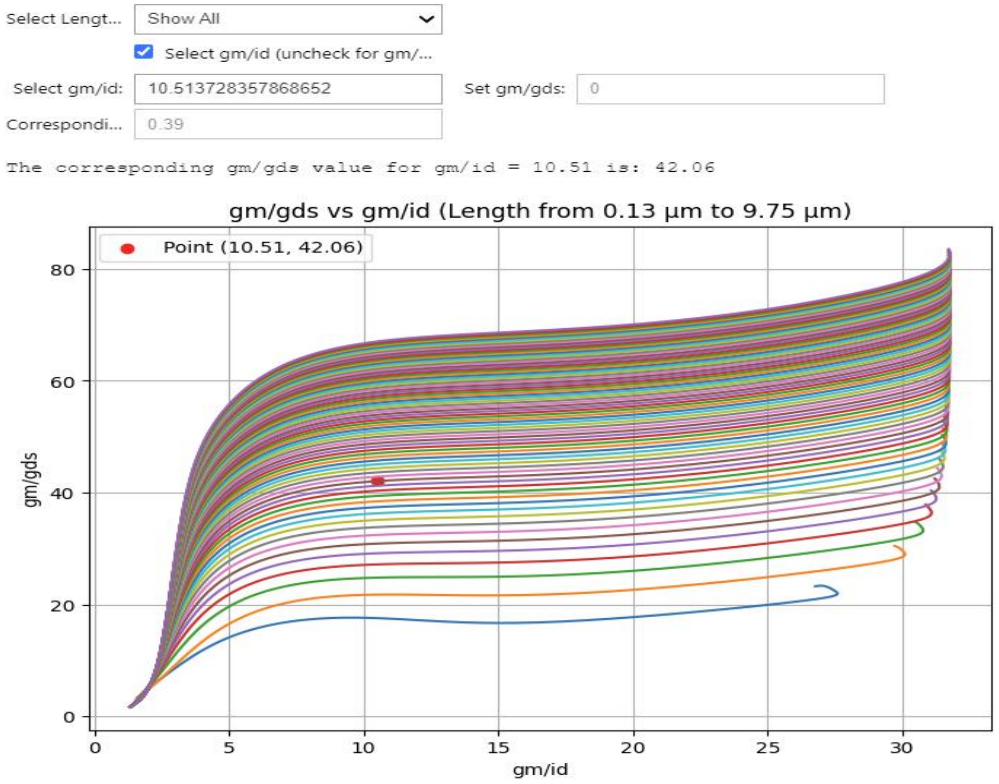
Klayout LVS ruledeck:

- accepts CDL netlist,
- extracts devices from layout,
- creates extracted netlist,
- performs checks and compares:
  - Pins
  - Nets
  - Devices
- reports inconsistencies
- can run in batch mode

OS tools for Advanced IC Design?

MOSFET Sizing with GM/ID Curves:

- Using Python scripting alongside Ngspice to generate GM/ID curves for efficient MOSFET sizing



Mixed Signal Design

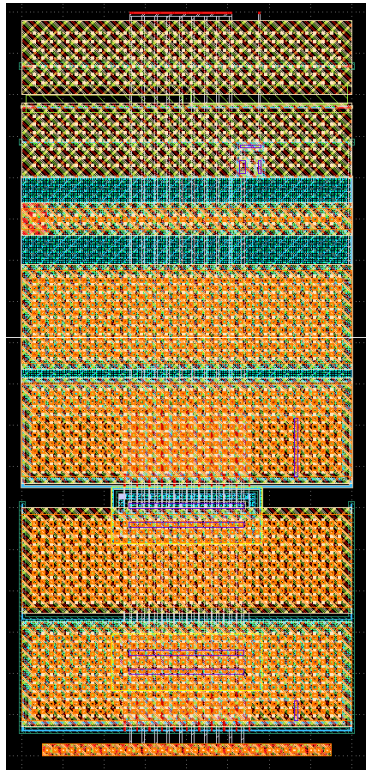
- Verilator
- Xspice
- Creating digital models in conjunction with analog design

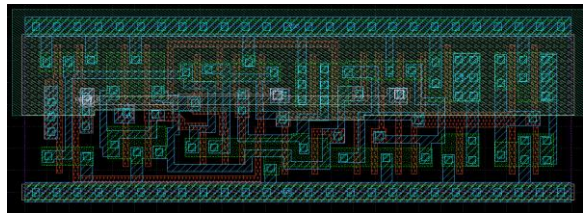
Layout Automation

- Physical verification, filler scripts
- Pcells generation from SPICE-Files
- Streamlining the layout process

Digital primitives

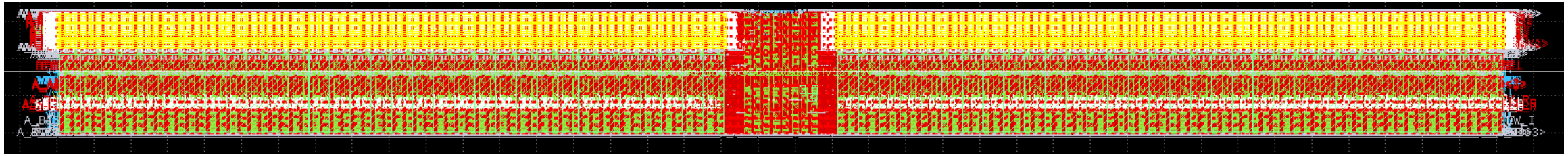
	StdCells	IOCells	SRAM
Verilog	x	x	x
LIB	x	x	x
LEF	x	x	x
CDL	x	x	x
SPICE	x	x	x
GDS	x	x	x



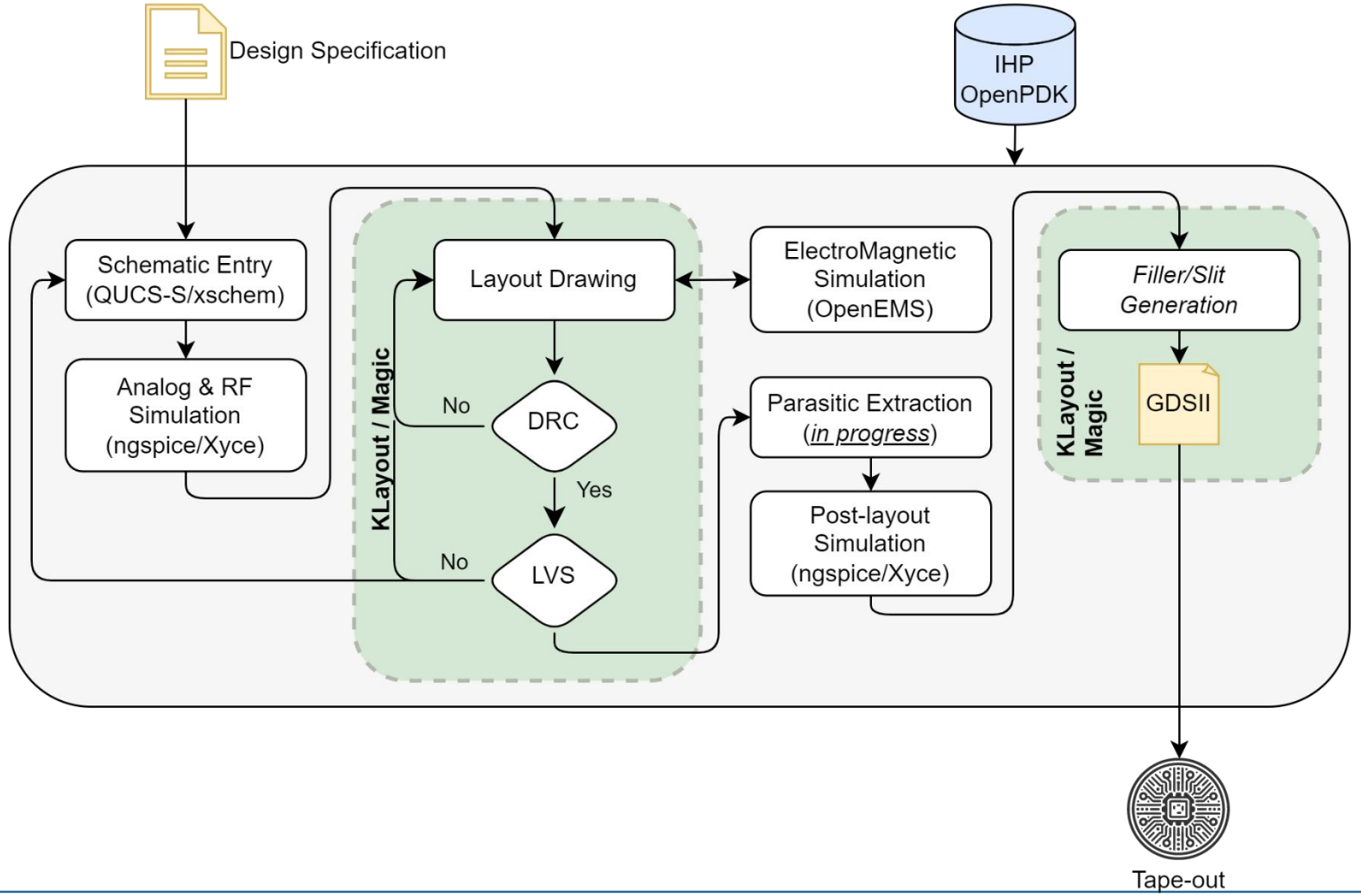


Digital components:

- stdcells
  - 84 cells,
  - combinatorial logic,
  - sequenntial elements,
  - scan flops,
  - gated cells.
- IOCells,
  - In, Out, InOut, Analog
  - different drive strengths
- SRAM
  - hard macros of a single port SRAM
  - different sizes

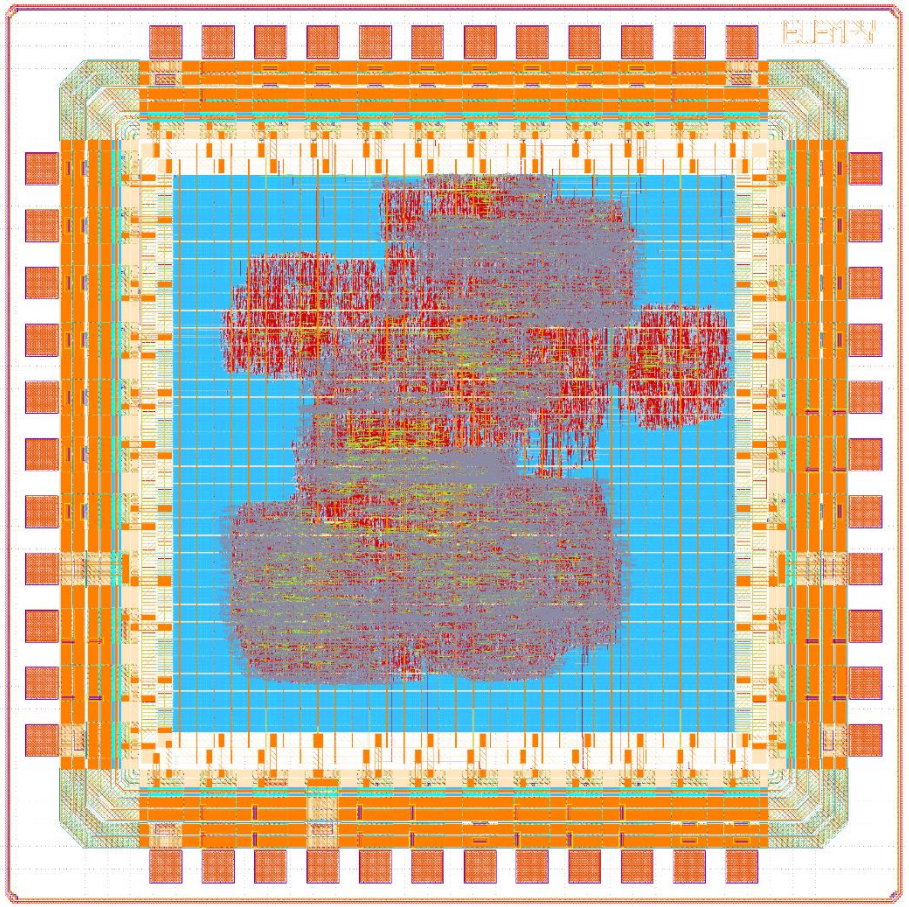


Analog/RF Open Source Design Flow: status at a glance

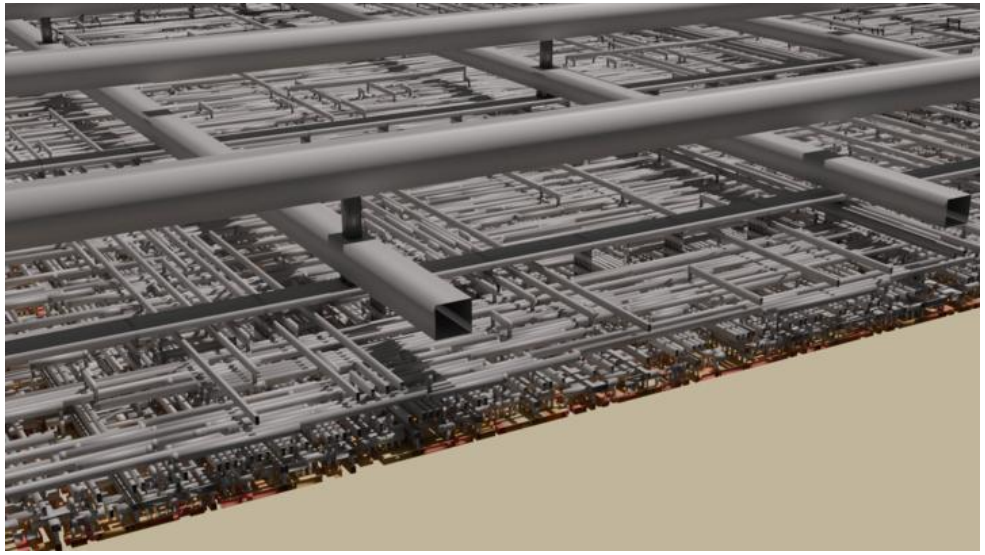


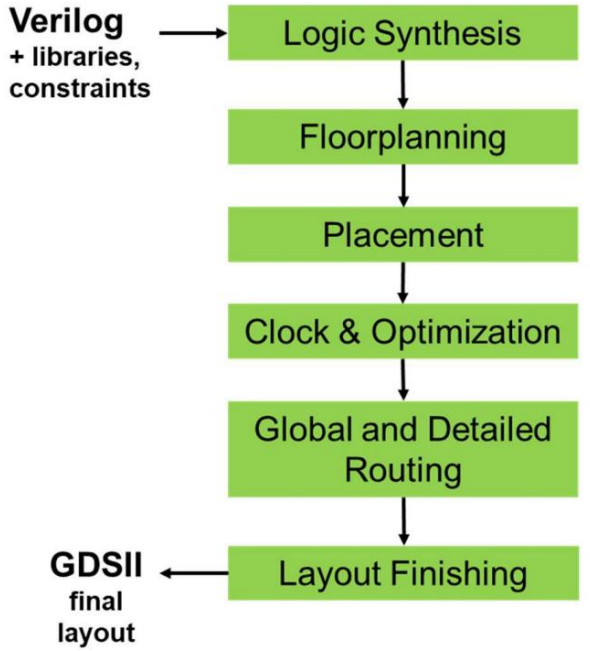
- KLayout-oriented flow
  - Layout design
  - Parameterizable cells
  - Physical Verification
- QUCS-S, xschem
- ngspice, Xyce
- OpenEMS, ElmerFEM, AWS Palace
- Working on a faster solver for EMS (ELMER)

Digital OpenROAD-flow-scripts Flow



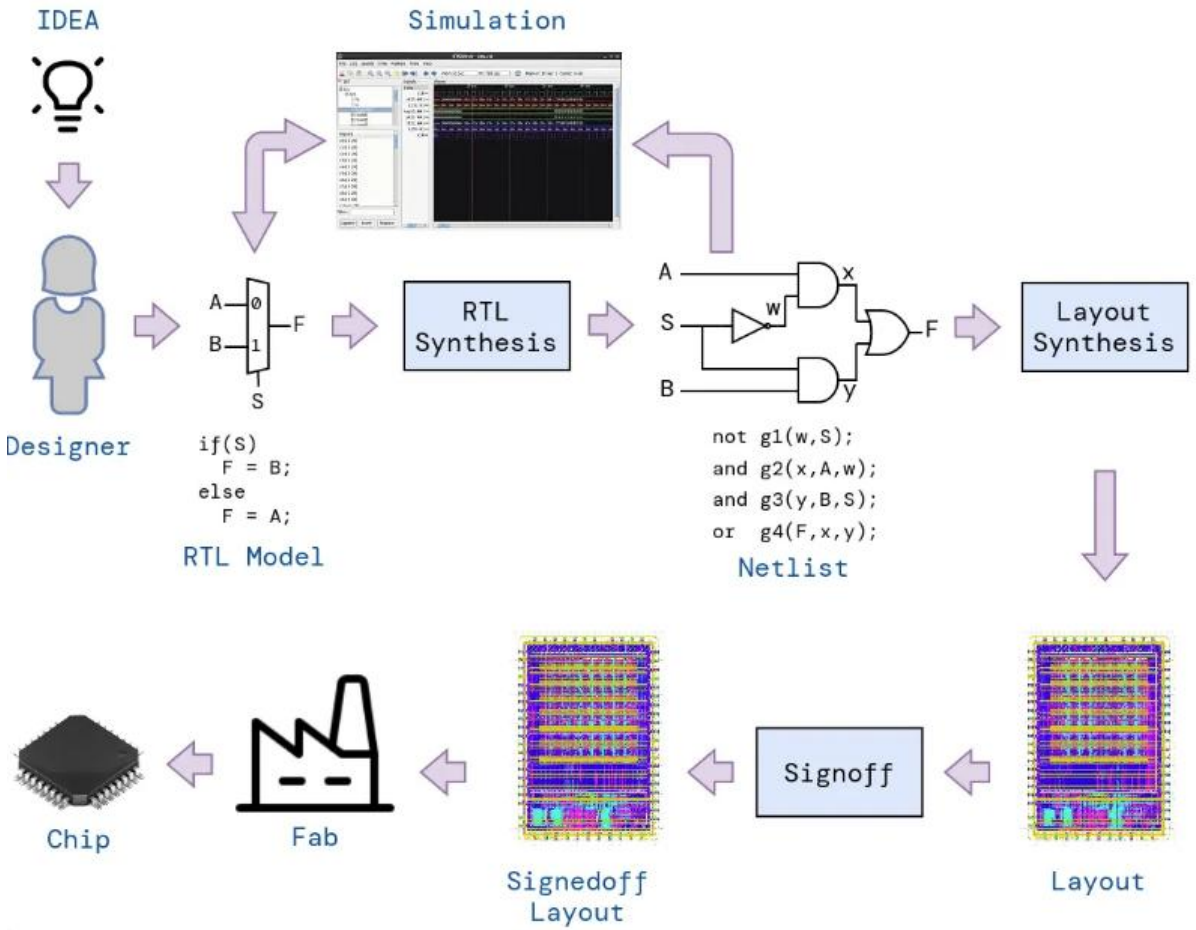
- Yosys + ABC - > synthesis
- OpenROAD -> PnR
- Klayout -> GDS streaming+checks

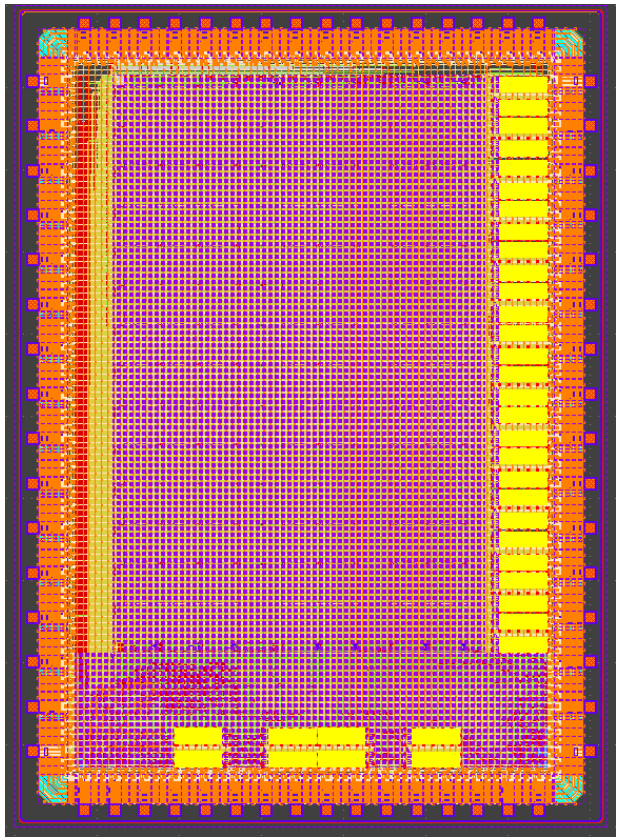


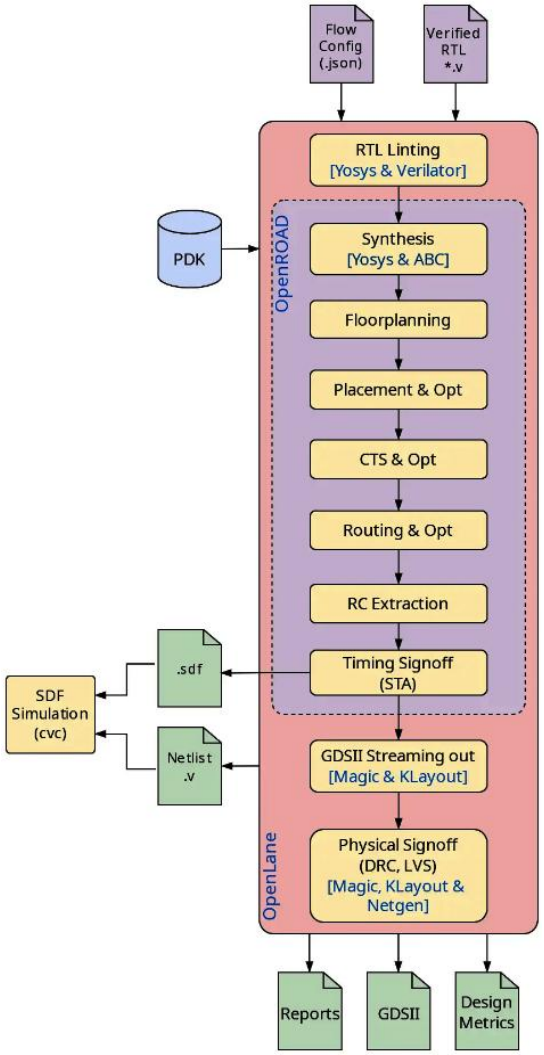


https://github.com/The-OpenROAD-Project/OpenROAD-flow-scripts

Digital LibreLane flow







https://github.com/librelane/librelane

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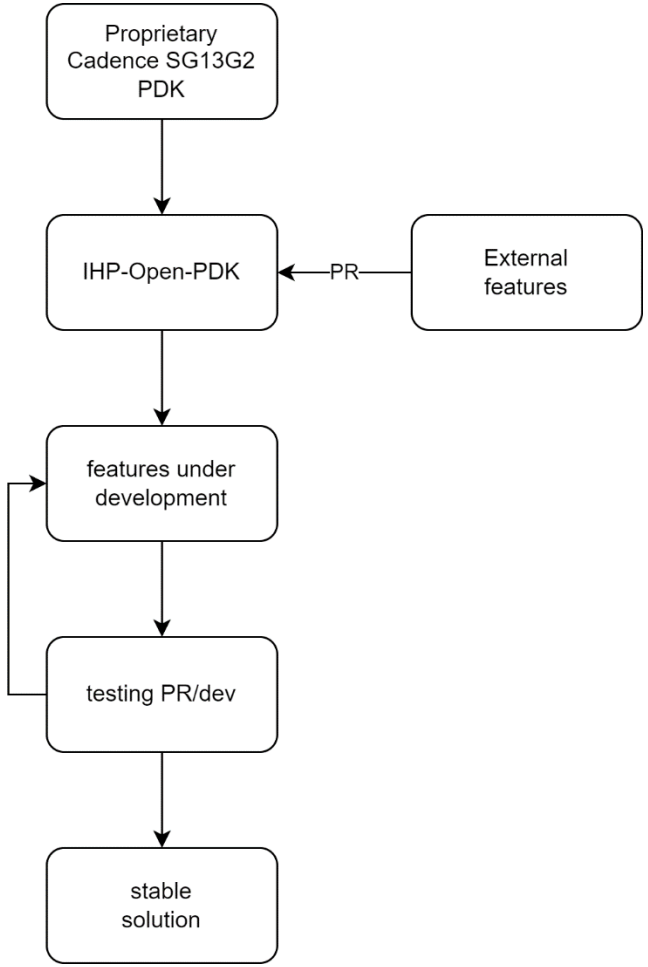
PDK development cycle

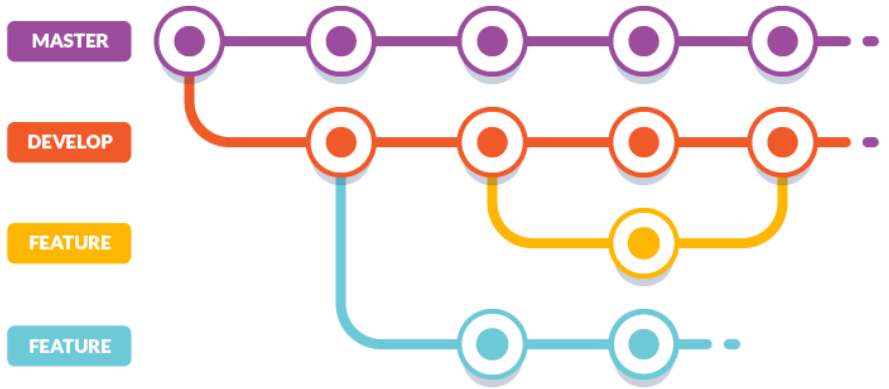


Principal rules

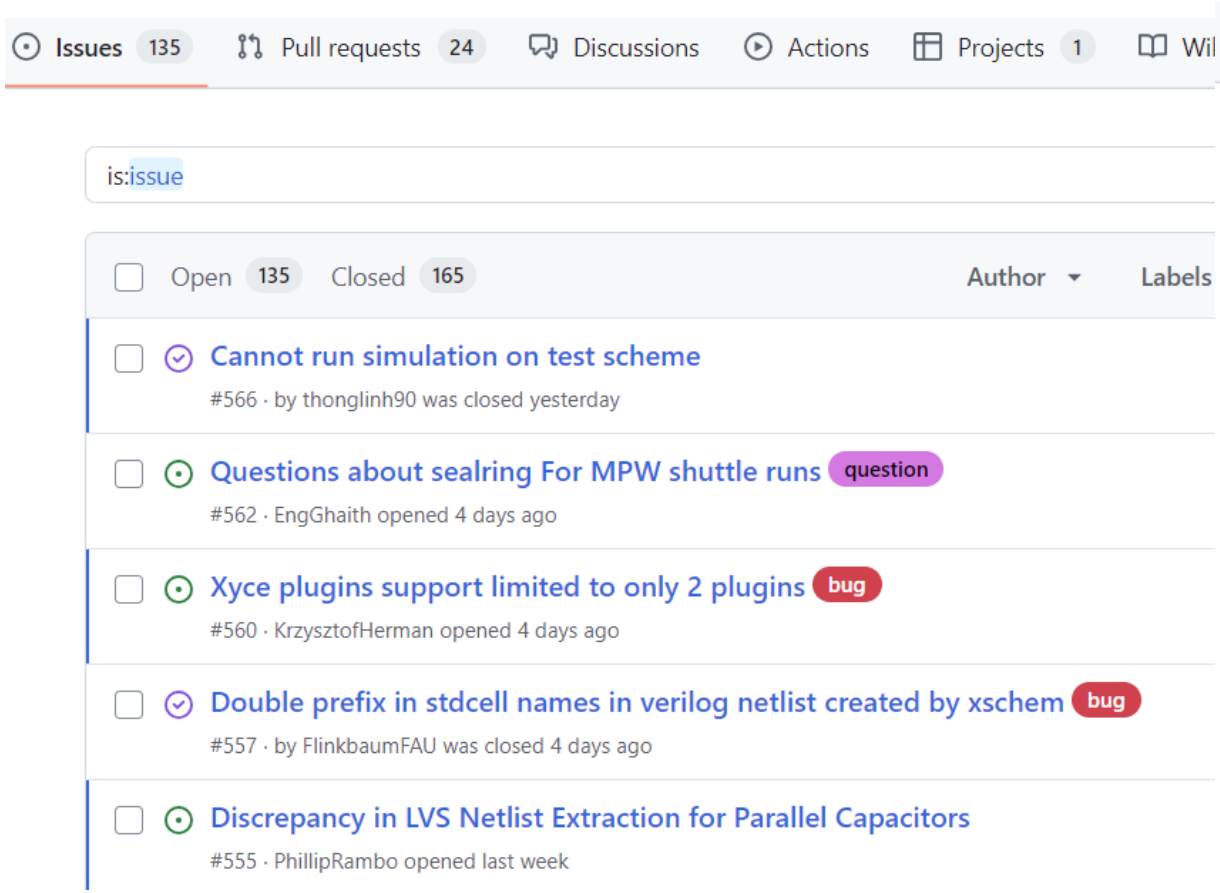
- Tight link between SG13G2 PDK and its open-source equivalent
- Compatibility with the open-source EDA tools
- Preserving the structure proposed in SKY130
- Read-only
- Based on git and following git flow

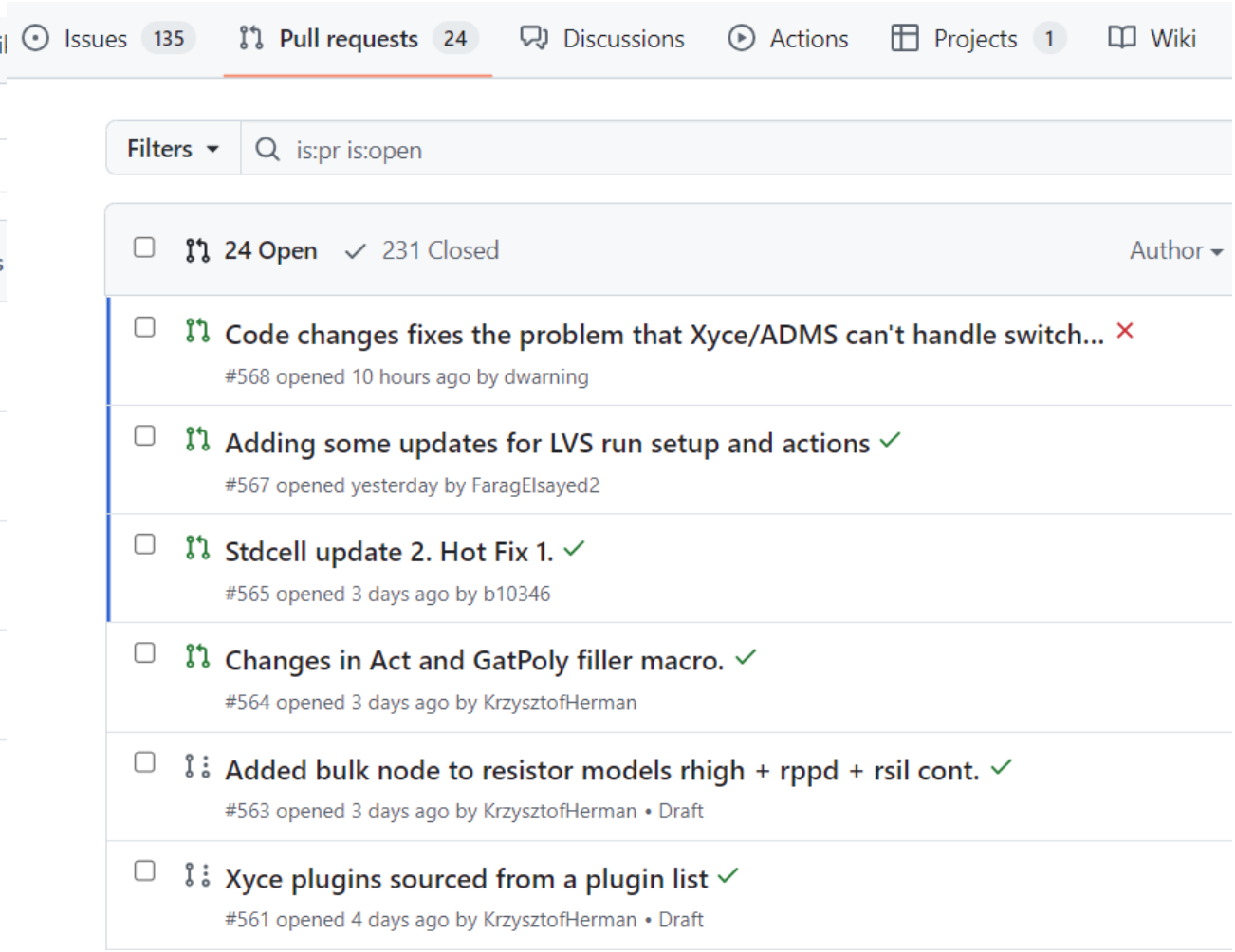
Key actors

- PDK core team
- Tools and flow developers
- Designers
- OS Community



PDK development cycle – community support





Work in progress – analog/mixed/RF flow

- Parasitics Extraction PEX – ongoing, https://github.com/martinjankoehler/klayout-pex
- Noise modeling in ngspice (transient noise, low frequency noise) – ongoing
- Qucs-S support – ongoing, agnostic PDK support, RF features
- Device models – issues found and reported by community members, migration to Verilog-A behavioral models
- New and fast DRC ruledeck for klayout
- OpenEMS integration for EM filed solving
- Mixed mode testcases using xspice + verilator

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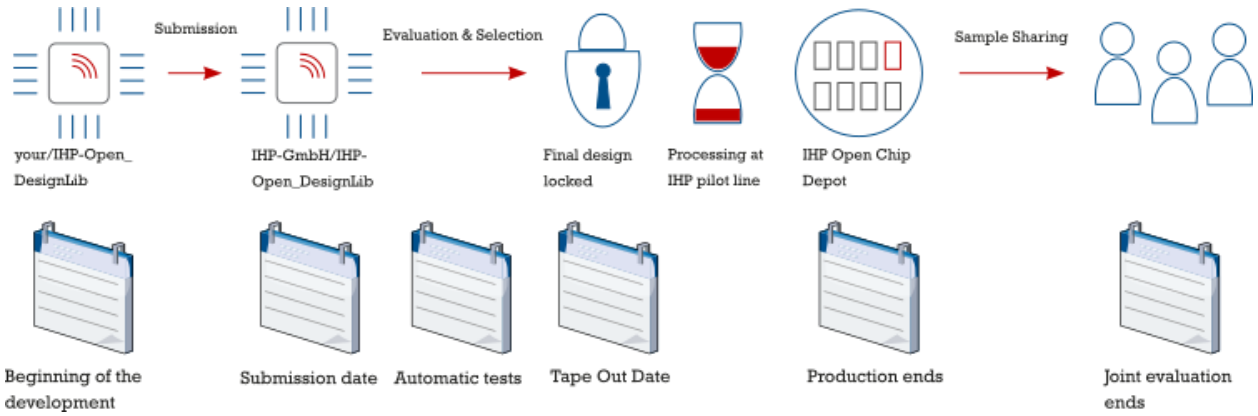
Free MPW Runs - support open source PDK & design

- The table provides schedule of MPW Runs for FMD-QNC project in 2025 and 2025

Tape out date	22/05/24	11/11/24	22/11/24	01/03/25	09/05/25	18/07/25	15/09/25
Technology	SG13G2	SG13CMOS	SG13G2	SG13G2	SG13G2	SG13G2	SG13CMOS
Area [mm^2]	10	220	20	140	30	30	220

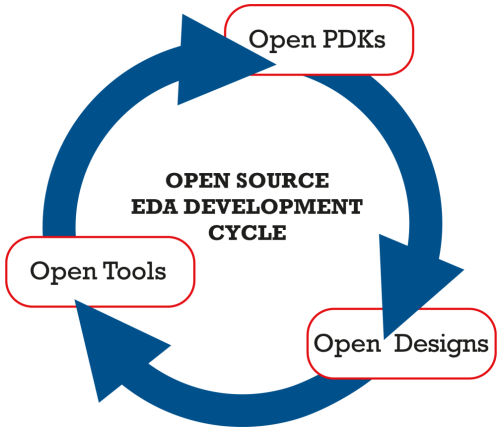
For more details check: https://ihp-open-ip.readthedocs.io/en/latest/

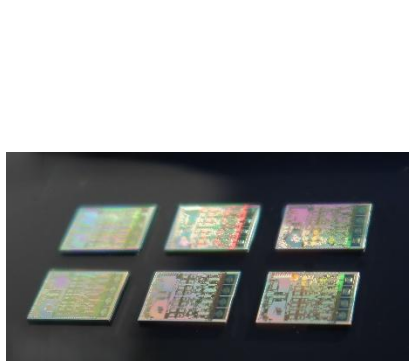


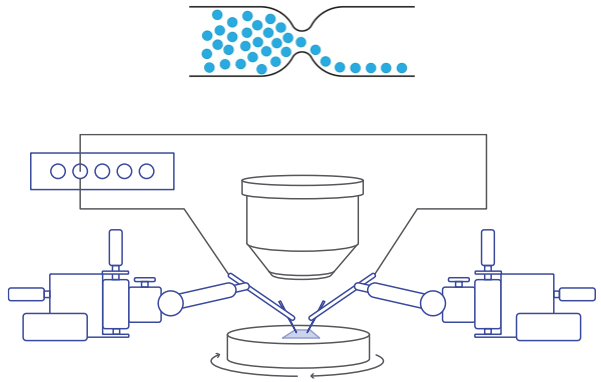
- Project funds can be used exclusively to produce chip designs for non-economic activities, such as university education, research projects, and others
- A concept for sustainable provision of free or low-cost MPW area for the open source community is to be developed.

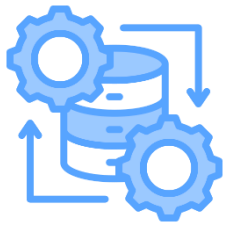
The future – Joint Evaluation

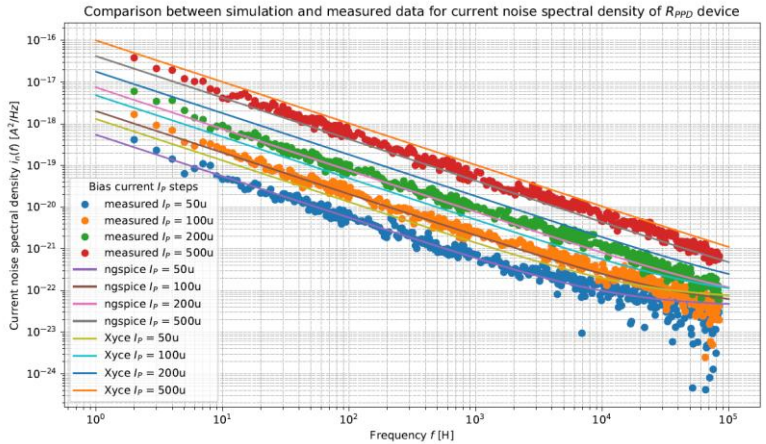
- Receiving your own silicon is just one milestone—it doesn't mean the development cycle is complete.
- The samples/wafers from free OpenMPW will be stored at IHP
- Anybody can rent chips for mesurments
- Silicon cross validation as research good practices
- Verified IP can become part of an open-source design library
- **How to organize the measurement to balance the load of the measurements lab ?**
- **How to organize the data processing ?**











The future – European Chip Design Platform with open-source

- Chips JU initiative
- Cloud based design environment with EDA tools, flows and IP's
- Open source is part of the platform: Analog, RF, AMS, Digital and Photonics related tools, flows
- Open-source design library: open source IP's

DCT

DET DET DET

EuroCDP

DET call is open right now – ChipFlow will apply so contact Rob Taylor for more details

The future - Low cost MPW

In order to maintain open source MPW IHP plans to have two OpenMPW runs per year

- SG13CMOS – CMOS only run with AL BEOL where price „P” in EUR is calculated based on total area (mm²) „A” booked

$$P = \begin{cases} - & if \quad A < 100 \\ 150000/A & if \quad 100 \leq A \leq 150 \\ 1000 & if \quad A > 150 \end{cases}$$

- SG13G2 – fully featured G2 with AL BEOL at approx. 2800 EUR/mm²

The above mentioned prices refer to the open-source designs, where all the views are compatible with the open source EDA tools.

For customers who do not wish to disclose their IP, we offer participation in the OpenMPW program at a 20% discount off the regular price, as the wafers can be shared with other customers.

The turn around processing time is approx. 6 months for CMOS - 8 months for BiCMOS

The typical offer includes 20 bare die samples. Packaging will be offered on request (additional fee can be applied)

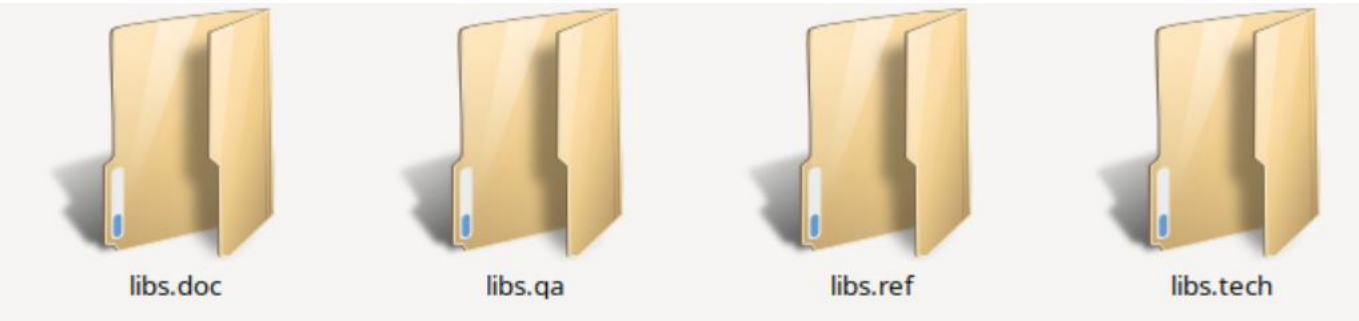
The first run can take place 24-th Nov 2025 (CMOS)

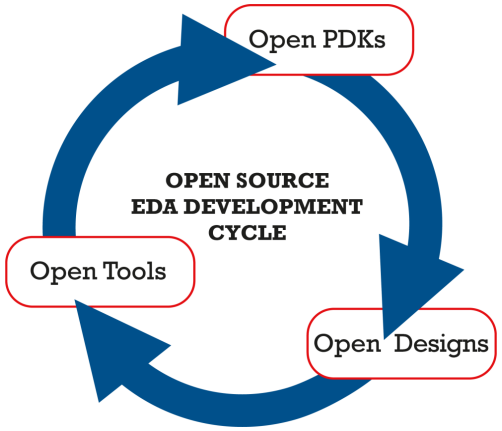
Table of contents

How do we make the IHP-Open-PDK ?

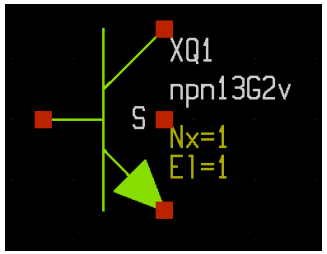
Key development rules of IHP-Open-PDK:

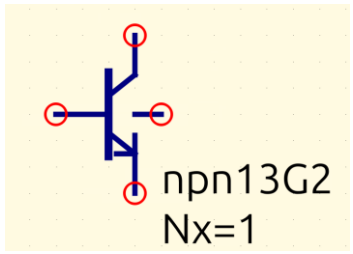
- Compatibility with technology – PDK is defined by technology
- Compatibility with the open-source tools (standarization, dependencies)
- Tight link between Cadence SG13G2 PDK and its open-source version
- Four+ eyes principle – review process

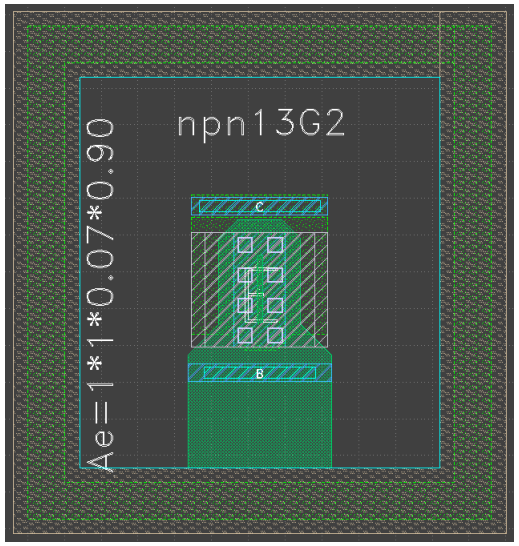




Device integration process







- $PDK_ROOT/$PDK/libs.tech/xschem/sg13g2_pr/npn13G2.sym
- $PDK_ROOT/$PDK/libs.tech/xschem/sg13g2_tests/
- $PDK_ROOT/$PDK/libs.tech/qucs-s/user_lib/IHP_nonlinear...*.lib
- $PDK_ROOT/$PDK/libs.tech/qucs-s/examples/
- $PDK_ROOT/$PDK/libs.tech/ngspice/model/cornerHBT.lib
- $PDK_ROOT/$PDK/libs.tech/xyce/model/cornerHBT.lib
- $PDK_ROOT/$PDK/libs.tech/verilog-a/vbic/vacode/vbic_1p3.va
- $PDK_ROOT/$PDK/libs.tech/klayout/python/sg13g2_pycell_lib/ihp
- $PDK_ROOT/$PDK/libs.tech/magic/ *ongoing
- $PDK_ROOT/$PDK/libs.tech/klayout/tech/drc
- $PDK_ROOT/$PDK/libs.tech/klayout/tech/lvs

Check list:

- Xschem symbol
- Qucs-S symbol
- Ngspice model
- Xyce model
- Verilog-A model
- Xschem example
- Qucs-S example
- Klayout PyCell
- Magic Pcell
- DRC -test
- LVS extraction rules
- LVS - test

Device model development

Current modelling approach:

- Based on Spice
- Partially supported by Verilog-A models via OSDI interface

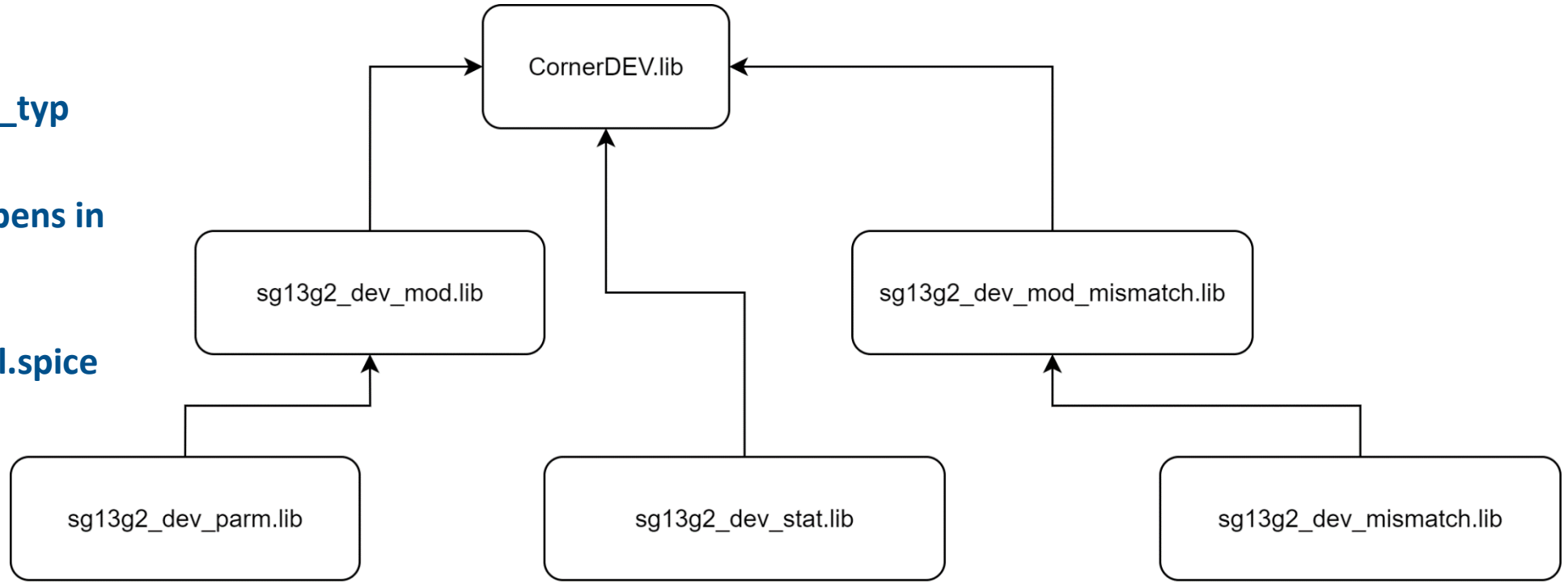
Corners:

- dev_typ, dev_bcs, dev_wcs, dev_typ_stat
- mos_tt, mos_ff, mos_ss, mos_fs, mos_sf, mos_tt_stat

.lib CornerDEV.lib dev_typ

The actual magic happens in $HOME/.spiceiinit

.include sg13g2_stdcell.spice



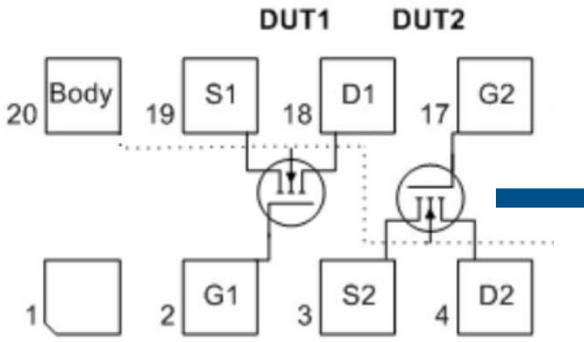
Device model development

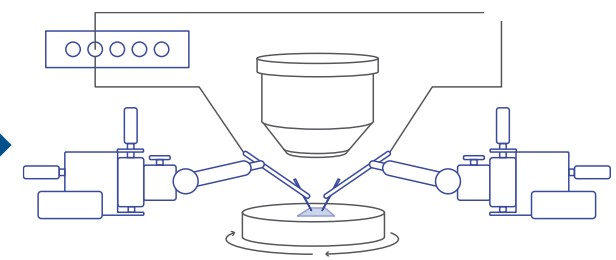
Current modelling approach:

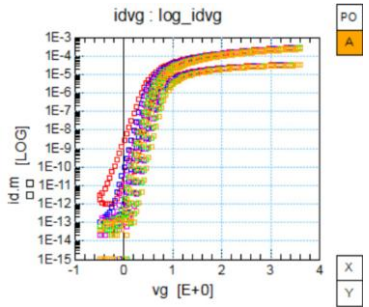
- Industrial flow uses Keysight ICCAP
- Measurements are taken for different conditions: temperature
- Multiple measurements -> statistics (process, global variation)
- Co-simulation spectre, hspice, ngspice

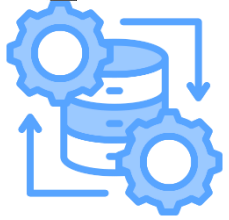
Alternative open-source flow:

- Device Modeling Toolkit by Semimod
- co-simulation with ngspice
- Verilog-A modelcards support









Parameter Extraction

```
.model npn13G2_NX_vbic npn
+ level = 9
+ vbe_max = 1.6
+ vbc_max = 5.1
+ vce_max = 1.6
+ tnom = 27
+ cbeo = '8.00E-16*(Nx*0.25)**0.975'
+ cje = '8.418E-15*(Nx*0.25)**0.975*vbic_cje'
+ pe = 0.92
+ me = 0.12
+ aje = -0.50
+ wbe = 1.00
+ cbco = '2.36E-15*(Nx*0.25)'
+ cjc = '1.53E-15*(Nx*0.25)*vbic_cjc'
+ pc = 0.558
+ mc = 0.12
+ ajc = -0.50
+ cjep = '3.56E-15*(Nx*0.25)*vbic_cjc'
```

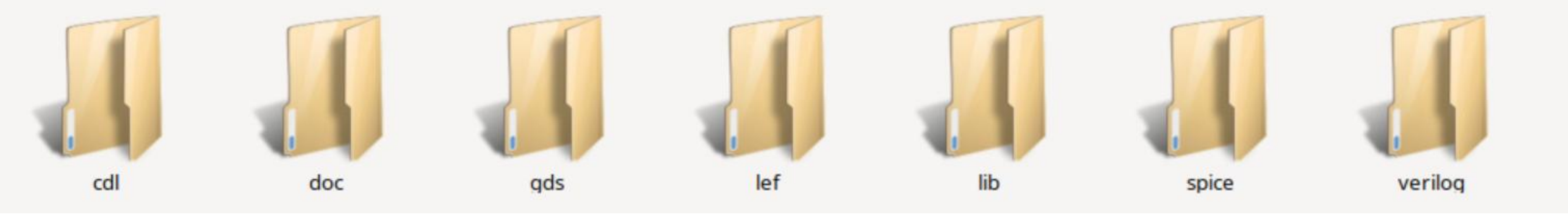
Standard cells development

Standard cells reverse engineering:

- GDS -> CDL
- CDL->SPICE
- SPICE->LIB
- CDL->Verilog
- GDS->LEF

Stdcell alternative open-source flow:

- Verilog
- Schematic/Spice netlist
- SPICE->LIB (lctime, libretto, CharLib)\
- SPICE->GDS lclayout
- GDS->LEF (Magic)

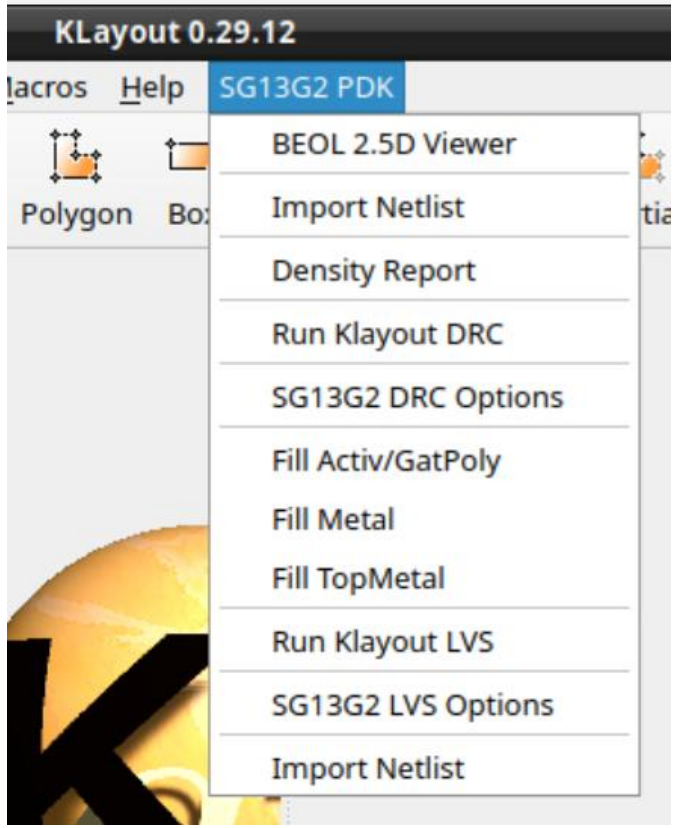


Physical verification is critical

- Klayout DRC rule deck is written in RUBY
- $PDK_ROOT/$PDK/libs.tech/klayout/tech/drc
- be careful when running DRC durring submission it is only a foundry precheck

- Klayout LVS rule deck is written in RUBY
- $PDK_ROOT/$PDK/libs.tech/klayout/tech/lvs

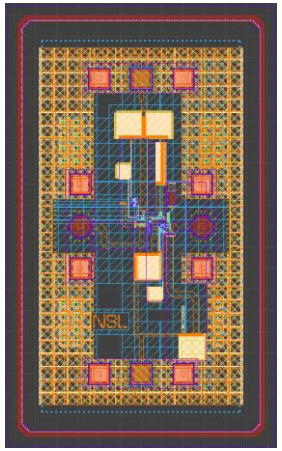
- performance – populate jobs on multicore up to 24
- be careful with RAM



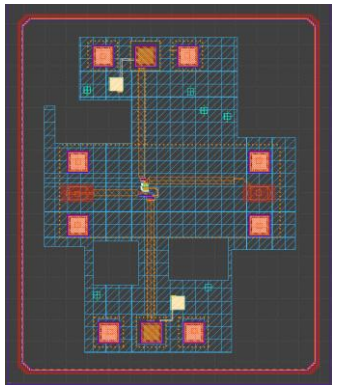
Open-source design library

In principle the Design Library does not exist yet but...

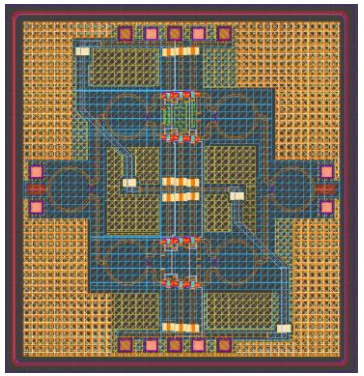
97 GHz TIA



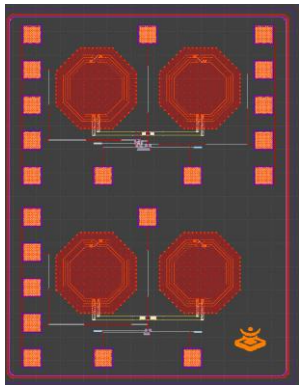
DC to 130 GHz TIA



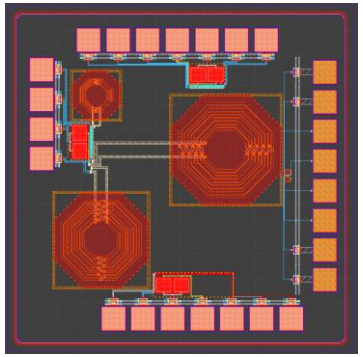
4-way 180 GHz PA



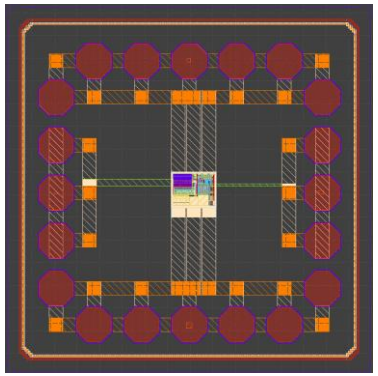
5GHz Mixer



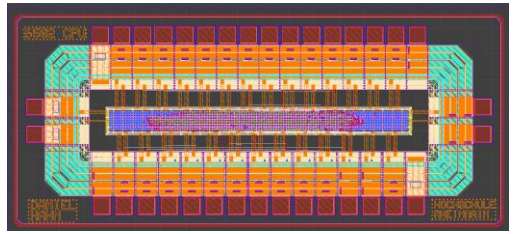
GPS LNA



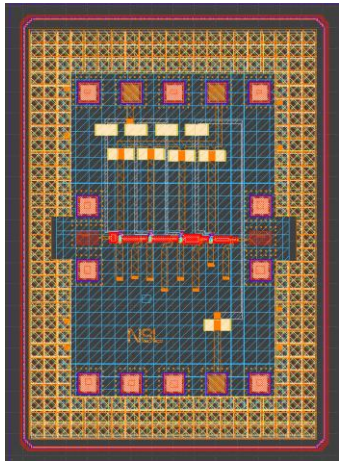
BG - Vref



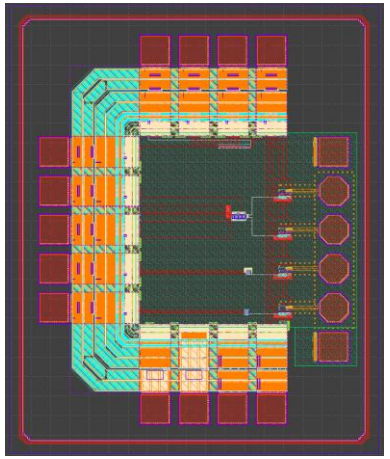
6502 cpu



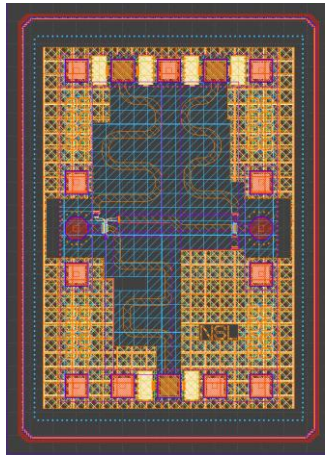
160 GHz LNA



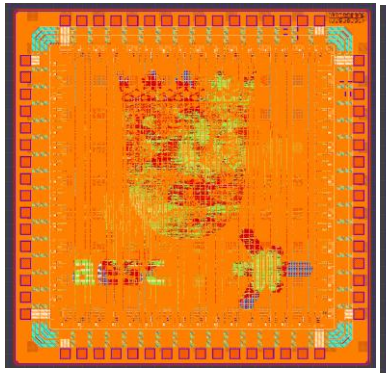
Active L VCO



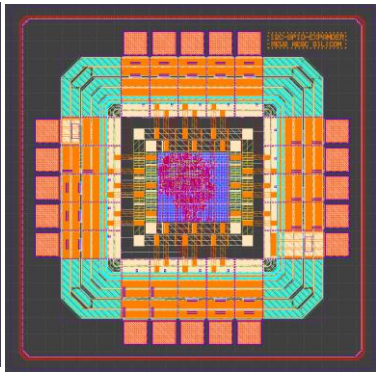
40 GHz LN TIA



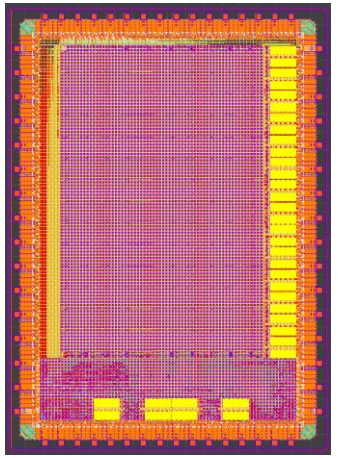
ElemRV-N



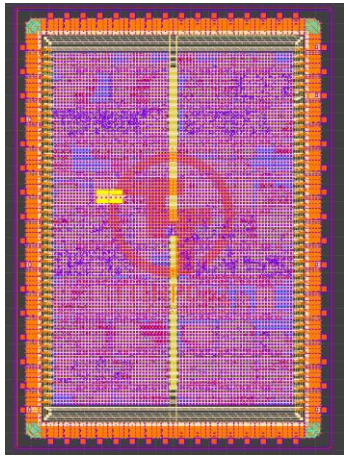
I2c-gpio-expander



Greyhound



2x TT



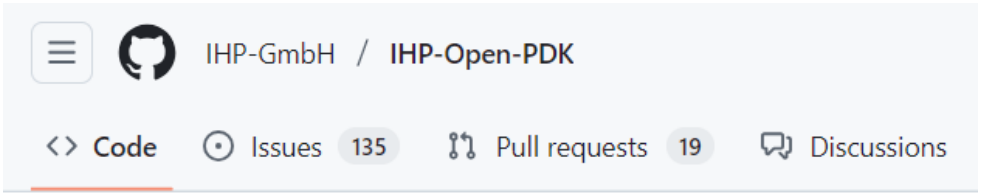
How to reach us

Email

- openpdk@ihp-microelectronics.com

GitHub

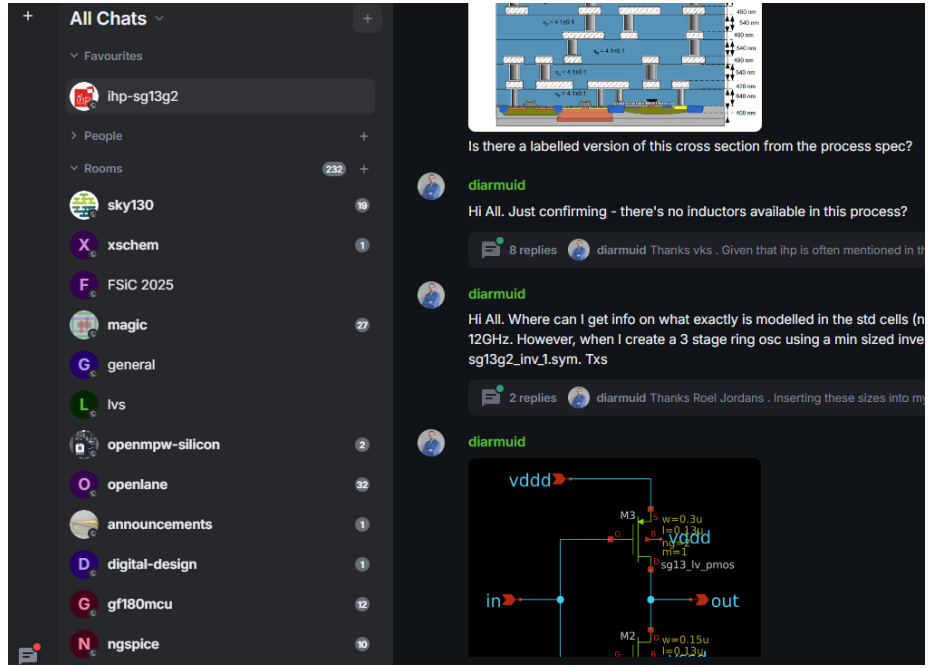
- issues – for reporting issues, questions
- discussions – for requesting features



Open Source Fossi-Chat.org channel:

`#ihp-sg13g2`

- general discussions
- announcements



Funding opportinities

https://nlnet.nl/

Amaranth HDL	Design FPGAs and ASICs in Python
Apicula IO primitives	Add additional IO primitives to libre Gowin FPGA tools
FABulous Demo SoC	SoC with open source FPGA based on FABulous
FPGA-ISP-UVC-USB2	Open hardware FPGA-based USB webcam
LiteX	Developer framework for FPGA and ASIC designs
LibreSilicon: Pad Cell Generator	Custom pad cells for integrated chip layout generation
Test Procedures for MOSFET SPICE Model Validation	
pcb-rnd, sch-rnd	Open source EDA suite

Send in your ideas. Deadline October 1, 2025

Acknowledgements

To BMFTR -> FMD-QNC (16ME0831) https://www.elektronikforschung.de/projekte/fmd-qnc

To our team at IHP

Join our team:
- open positions
- student's internship

To all members of the open-source community who have supported and contributed our initiatives

Thank you for your attention!

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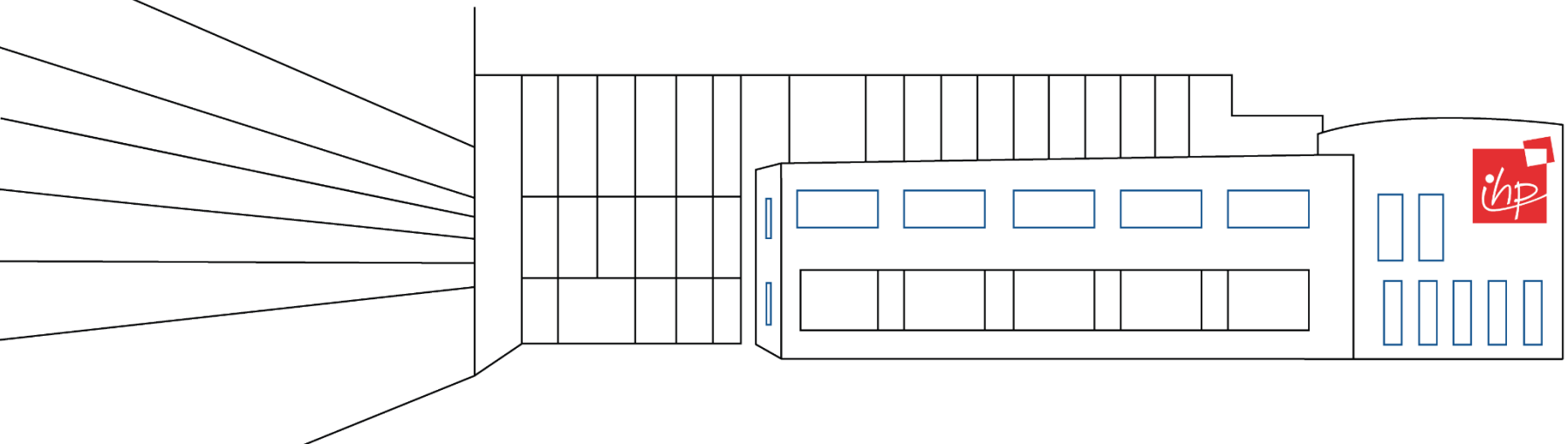
E-Mail: herman@ihp-microelectronics.com



Leibniz Association